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Hybrid optical integrator based on silicon-on-insulator platform

A Thesis

Submitted to the Faculty

of

Rose-Hulman Institute of Technology

by

Taewon Huh

In Partial Fulfillment of the Requirements for the Degree

of

Master of Science in Optical Engineering

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ROSE-HULMAN INSTITUTE OF TECHNOLOGY

Final Examination Report

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Graduate Major

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PASSED X　　**FAILED** ____

ABSTRACT

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Rose-Hulman Institute of Technology

February 2019

Hybrid optical integrator based on silicon-on-insulator platform

Thesis Advisor: Dr. Azad Siahmakoun

A hybrid optical integrator is a recirculating loop that performs oversampling typically for analog input, using the cross-gain modulation (XGM) in a semiconductor optical amplifier (SOA). The modulated input signal changes the gain of the loop through XGM and thus modifies the loop accumulation. This thesis presents hybrid optical integrator for an all-optical analog-to-digital converter based on a silicon photonics platform. The device consists of silicon waveguides of dimension 220 × 500 nm (thick × width) and approximately 5 m optical loop length including fiber length, input and output grating couplers for 1550 nm signal, directional couplers, and external components (SOA, optical isolator and band-pass filter). The silicon photonics devices are designed for fabrication on the SOI wafer using E-Beam lithography. Fiber-optic integrator and hybrid optical integrator are constructed to demonstrate and evaluate a theoretical model for the system. The system is characterized for square waves at Mega-Hertz input frequencies. Experimental results show a sampling period of 28 ns and free spectral range of 35.7 MHz with an optical loop length of five meters, which is in excellent agreement with the theoretical model of the leaky integrator.

Keywords: Hybrid Optical Integrator, FSR, Oversampling, SOI, SOA, Sampling Frequency

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LIST OF ABBREVIATIONS

AFM	Atomic Force Microscopy
A/D	Analog to Digital
BOE	Buffered Oxide Etch
BPF	Band-Pass Filter
CW	Continuous Wave
DRC	Design Rule Check
DSM	Delta-Sigma modulator
EAM	Electro-Absorption Modulator
EIM	Effective Index Mode
FSR	Free-spectral Range
FDTD	Finite-difference Time Domain
GDS	Graphic Database System
I/O	Input/Output
OC	Optical Coupler
OSA	Optical Spectrum Analyzer
PDK	Package Design Kit
RMS	Root Mean Square
RF	Radio Frequency
SEM	Scanning Electron Microscopy
SOA	Semiconductor Optical Amplifier
SOI	Silicon-On-Insulator
TE	Transverse Electric
TM	Transverse Magnetic
XGM	Cross-Gain Modulation

LIST OF SYMBOLS

English symbols

$\boldsymbol{C}$	Coupling coefficient
$\boldsymbol{c}$	Speed of light in vacuum
dB	Decibel
$\boldsymbol{ed}$	Etch depth
$\boldsymbol{f_B}$	Band-limited Frequency
$\boldsymbol{f_N}$	Nyquist Frequency
$\boldsymbol{f_S}$	Sampling frequency
$\boldsymbol{G}$	Gain of SOA
Hz	Hertz
$\boldsymbol{h[n]}$	Impulse response function in discrete-time domain
$\boldsymbol{I}$	Intensity of optical signal
K	Periodicity of the grating
$\boldsymbol{k}$	Coupling intensity coefficient of optical coupler
$\boldsymbol{k}$	Wave vector
$\boldsymbol{L}$	Optical loop length
$\boldsymbol{L_x}$	Crossover length
$\boldsymbol{m}$	Mode order
$\boldsymbol{n}$	Refractive index of material
$\boldsymbol{n_{eff}}$	Effective refractive index of material
$\boldsymbol{P}$	Power of light
$\boldsymbol{q}$	Quantized signal
$\boldsymbol{T}$	Sampling period
$\boldsymbol{t}$	Time domain

t	Coupling coefficient of through port
t	Oxidation time
$u[n]$	Unit step function
V	Voltage
w	Grating width
x_i	Initial oxide thickness
x_{ox}	Oxidation thickness
x	Input signal
y	Output signal

Greek Symbols

β	Propagation constant
Δ	Difference between input and output signal
θ	Angle between the surface normal and the propagation direction of light
κ	Coupling coefficient of cross-port
Λ	Grating period
λ	Wavelength
Σ	Input summing junction
τ	Time delay
ω	Signal frequency

1. INTRODUCTION

The state-of-the-art in silicon photonics has received a great deal of attention and has been developed as a key technology for the next generation signal processing system. The theoretical advantage of silicon photonics includes high-speed processing, high sampling rate, large bandwidth, and high level of integration, has led to significant research over the last decade. Although there has been outstanding solutions and achievement in the electronic signal processing, the potential of integrated silicon photonics is a promising technology that satisfies the demand for higher data processing speed with larger data capacity, lower power consumption, and low manufacturing cost [1]–[4]. In particular, all-optical analog-to-digital (A/D) conversion requires higher sampling rates at both optical and radio frequency (RF) domain, facilitating large bandwidth to avoid the electronic bottleneck [5]. Recently, several methods are suggested to reach GHz range sampling rate for A/D conversion, and a photonic delta-sigma modulator using oversampling technology is one of the practical solutions to compensate for the disadvantage of the electronic device [5]–[7]. One of the critical components of a delta-sigma modulator is an optical integrator where its sampling frequency and oversampling ratio have significant impacts on quantization and demodulation. The sampling frequency and oversampling ratio are related to the gain and time constant of the optical integrator, which defines the characteristics of device performance such as signal-to-noise ratio, spur-free dynamic range and effective number of bits [2], [8]–[10].

In this thesis, I present a hybrid optical integrator, constructed with silicon photonics and fiber-optic devices. The proposed system is based on the inverted optical leaky integrator and constructed which is experimentally verified by two systems: one with all fiber optics components and the other with a combination of fiber optics and silicon photonics. The main purpose of this

work is to demonstrate and evaluate the performance of the hybrid optical integrator and show that a silicon photonics chip can be a replacement of the fiber-optic system. By introducing silicon photonics device in the fiber-optics system, it is expected to increase the sampling frequency and oversampling ratio due to the reduction in the optical path. This will critically impact the system performance of the optical integrator and the delta-sigma modulator. In theory, a decrease of the optical path length of the integrator loop and an increase in the effective refractive index increases the free-spectral range (*FSR*), which in turn will affect the sampling frequency of the system [1]. Instead of constructing an optical loop with optical fibers, the optical loop with silicon waveguide decreases the loop length from meters to millimeter scale, providing a possibility for GHz sampling rate. Furthermore, silicon photonics has the potential for integrating multiple functions at a single package using CMOS manufacturing techniques common among advanced microelectronics industry [11].

To avoid interference within the integrator loop, two operating wavelengths are used, one for the input signal and the other for the accumulating signal. The circulating signal in the loop is selected by the cross-gain modulation (XGM) effect of a semiconductor optical amplifier (SOA) and a band-pass filter. In addition, it becomes easier to control the gain and delay time by adjusting the driving current of the non-linear SOA in the integrator. Furthermore, the operation of the hybrid optical integrator is based on controlling the gain of the SOA, which provides the possibility of a complete integrated device to be fabricated by silicon photonics technology.

First, a mathematical model of the optical integrator system is developed based on the theoretical description of the optical integrator. Then, the components of the silicon photonics

(SiPh) devices are designed based on a Silicon–on–Insulator (1 cm × 1 cm) platform. The SiPh components in each device are designed and optimized at the operation wavelength using simulation software 'Lumerical.' The silicon photonics passive device includes a waveguide, four grating couplers, two directional couplers, and two Y–Branches that are patterned by E-beam lithography. To prevent cross-talk noise and multi-polarization modes of the input light source, a waveguide with 220 nm thickness and 500 nm width is used to only select and pass fundamental transverse electric (TE) mode. The performance of the proposed device is investigated and compared with simulation results by acquiring the output signal for a square-shaped input signal of various frequencies. The sampling period and free-spectral range (FSR) of the device are determined by analyzing the output signal.

2. THEORY

In this Section, we discuss the background and theory of an optical integrator and its passive SiPh components for a Delta-Sigma Modulation. The mathematical model of an optical integrator is presented, and the operation principle is provided with simulation result. Then, the mathematical model and design method for the passive SiPh components, such as a grating coupler, directional coupler, and Y–Branches are presented. The detailed setup for the Lumerical simulation of grating coupler is described in Appendix A. The theoretical model of the integrator and its result will be compared with the experimental results of the fabricated device and discussed in Section 4.

2.1 Overview of Delta-Sigma Modulator

The general Analog-to-Digital Converter (ADC) operation can be characterized by the four distinct function blocks shown in Figure 2.1(a), including a pre-filter, a sampler, a quantizer, and an encoder [1]. The operation of general ADC can be described by following an input signal as it progresses through each element shown in Figure 2.1. First, the analog input signal $x(t)$ is pre-filtered at the band-limited frequency f_B to avoid aliasing that could occur during the subsequent sampling operation. Then a sampler is adapted to acquire information about the continuous amplitude of the input signal at discrete time intervals of a sampling period. A proper sampling frequency, f_S, is chosen to satisfy the Nyquist criterion for the signal recovery where $f_S = f_N = 2f_B$. From the sampling theory, the sampling frequency must be at least twice the f_{max} of the input signal in order to recover a sampled signal $x(nT_S)$ without distortion or loss of information. There are other sampling methods for the specific applications, such as sub-sampling ($f_S \ll f_N$) and

oversampling ($f_S \gg f_N$). After the sampler, quantization of the sampled input is processed, convert a full-scale amplitude range into a small sub-range amplitude. Finally, the quantized signal $q(nT_S)$ is generated into a form of digital code $y(nT_S)$ by a digital processor or encoder [1], [2].

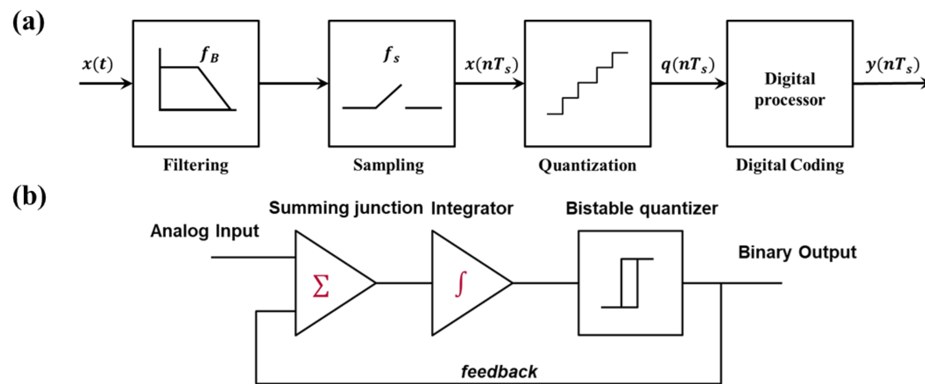


Figure 2.1: Block diagram of the process of (a) general ADC, and (b) first-order Delta-Sigma modulator. *x*(t) is a continuous analog input signal, and *y*(*nTs*) is a binary output signal.

The Delta-Sigma Modulator (DSM) is a part of the ADC architectures that uses oversampling of an input signal higher than the Nyquist criteria, f_N [12], [13]. Figure 2.1(b) shows the block diagram of the DSM. The function of DSM is encoding the analog input signal into the binary stream. The feedback loop is applied to reduce the error of conversion, where feeding the output signal back to the input summing junction (Sigma Σ) to measure the difference between the input and output (Delta Δ) and using it to improve output signal quality. Different from the general ADC technique that uses a sampling frequency equal to Nyquist frequency, the sampling frequency of DSM is higher than the Nyquist frequency ($f_S \gg f_N$). The oversampling provides a reduction of noise in the band of interest, avoiding the use of high-precision analog circuits for the anti-aliasing filter, and quantization noise shaping [12]. This work is focused on the optical leaky integrator,

functioning as an integrator of DSM in Figure 2.1(b). Depending on the system properties, the input frequency, or operation frequency, is decided (pre-filter) for the sampling to be appropriate for the further steps in ADC or DSM. The detailed theoretical model and the operation principle of the optical integrator will be discussed in Sections 2.2 to 2.4.

2.2 Optical Leaky Integrator

This section presents an optical leaky integrator for an optical A/D converter based on DSM. The optical integrator is a fundamental component in signal processing that can be worked as a filter, a pulse shaper, and a feedback control loop, and a component of delta-sigma modulator. In the application of DSM, the critical characteristics of the optical integrator for the system are the operation frequency and oversampling ratio. These two parameters can affect and define modulator performance by affecting the signal-to-noise ratio and spur-free dynamic range, which in turn depends on the gain and time constant of the optical integrator. It is essential to control these parameters and predict the performance of the modulator in order to design a system. The following contents describe the theoretical model of the optical leaky integrator based on an active loop with a non-linear semiconductor optical amplifier (SOA) and the operation principle in detail. The proposed optical integrator works with two wavelengths, an input wavelength and an accumulating wavelength in the loop to prevent inherent interference by two signals. The integration constant and the delay time are controlled by adjusting the SOA gain, which can be modified by the driving input current of SOA. A brief introduction to the SOA will be given to aid in the understanding of the operation principle of the optical integrator.

The SOA is an amplifier that increases the amplitude of an input optical signal by a stimulated emission process under a sufficient external injection current [14]. The schematic diagram of the SOA structure is given in Figure 2.2(a). The basic operation principle of the SOA is the same as a laser but without feedback. The difference between a laser and the SOA is that the end mirrors are replaced with anti-reflection coatings where feedback is suppressed. The optical gain of the SOA can be accomplished by pumping the SOA electrically or optically to achieve a population inversion. The optical gain depends on the incident signal frequency ω and the local beam intensity inside the amplifier. Carriers from an external bias circuit are injected into the active region of the SOA where they are confined by layers of materials with higher energy band gap (see Figure 2.2(b)) [14]. An optical signal impinging on the active region will induce simulated emission and will be amplified under the condition of population inversion (i.e., when the bias current is sufficiently large). The core of an optical waveguide in the SOA acts as a gain region where the refractive index is larger than that of the cladding. The propagating signal is confined within the waveguide, and amplified signal by population inversion can be acquired at the output port.

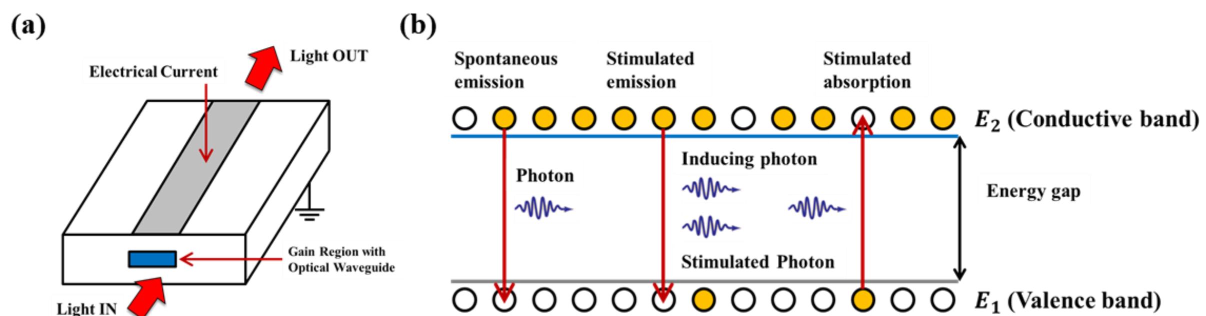


Figure 2.2: (a) Schematic diagram of an SOA structure and (b) spontaneous and stimulated process [14].

The optical integrator is based on an inverted leaky integrator, which accumulates positive input intensities, but gradually leaks a small amount of the input simultaneously [3]. A mathematical description for the integrator related to inverted leaky integrator can be used to specify the model parameters that define the characteristics and performance of the integrator [2], [8]. First, a discrete leaky integrator can be described by the equation given below:

$$y[n] = \tau y[n-1] + gx[n]$$

$$= \tau^{n} y[0] + g \sum_{k=0}^{n-1} \tau^{k} x[n-1] \tag{2.1}$$

where x and y are input and output signals, and g and τ are real constants where $g > 0$ and $\tau > 0$, with $n \geq 1$. The z-domain transfer function can be expressed as follows:

$$H_{LI}(z) = \frac{g}{1-\tau z^{-1}} = g \sum_{k=0}^{\infty} \tau^{k} z^{-k} \tag{2.2}$$

where z is the transform variable defined by $z = \exp(j\omega T)$, with the sampling period of the integrator T and angular frequency ω where the region of convergence is $|z| > |\tau|$. According to Eq. (2.2), the impulse response can be defined in terms of the unit step function u[n] as

$$h_{LI}[n] = g\tau^{n} \mathrm{u}[n] \tag{2.3}$$

In the case of a discrete inverted leaky integrator, a different equation can be defined to describe its mathematical model as

$$y[n] = a + \tau y[n-1] - gx[n]$$

$$= a \frac{1-\tau^{n+1}}{1-\tau} + \tau^{n} y[0] + g \sum_{k=0}^{n-1} \tau^{k} x[n-1] \tag{2.4}$$

where x and y are the input and output signal in Eq. (2.1) while a, g and τ are real constants which satisfy $0 < \tau \leq a$ and $0 < \tau < 1$. Contrary to Eq. (2.1), the above equation does not represent discrete, linear and time-invariant system due to the existence of constant a. Due to time-variance and non-linearity, Eq. (2.4) cannot be characterized by the impulse response and transfer function as previously done unless a equals zero. If a is assumed to be zero, the system can be described by the z-transfer function and the impulse response as shown in the equations below.

$$H_{LI}(z) = \frac{-g}{1-\tau z^{-1}} = -g \sum_{k=0}^{\infty} \tau^k z^{-k} \quad (2.5)$$

$$h_{LI}[n] = -g\tau^n \mathrm{u}[\mathrm{n}] \quad (2.6)$$

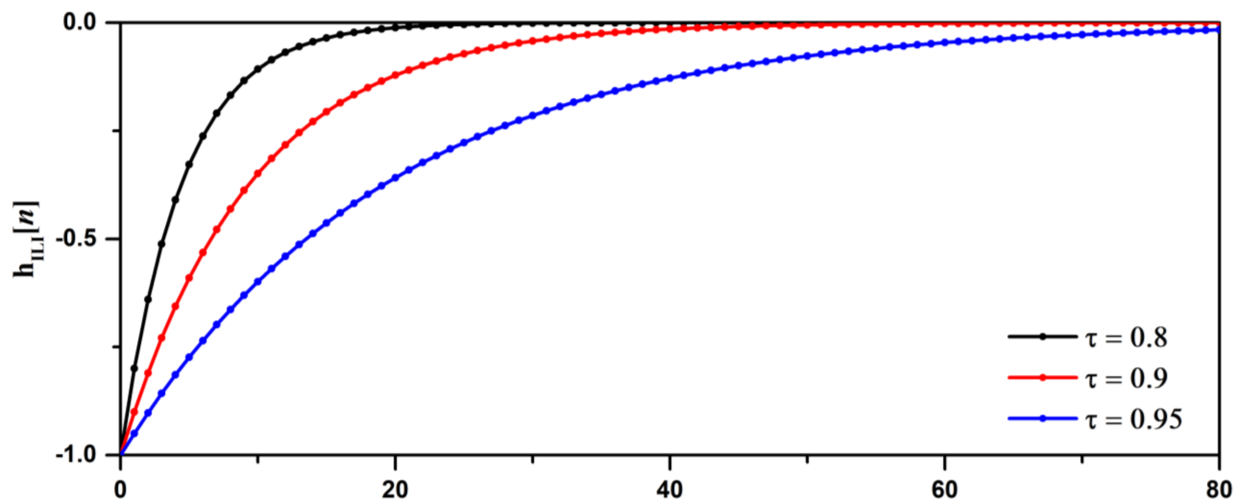


Figure 2.3: The impulse response of the inverted leaky integrator for different τ value.

Figure 2.3 shows the impulse response (Eq. 2.6) of an inverted leaky integrator for different values of the constant τ. As the value of τ increases, the impulse response maintains low values for longer time intervals. This indicates that the output signal of the integrator will depend on less number of the sampled input signal. Figure 2.4 shows the response of a leaky integrator for a

square-shaped input signal based on the Eq. (2.4). An optical integrator is designed based on the basic characteristics of the optical leaky integrator. Then, the system is evaluated theoretically and experimentally to determine if the performance of the system can be considered as a leaky integrator for DSM.

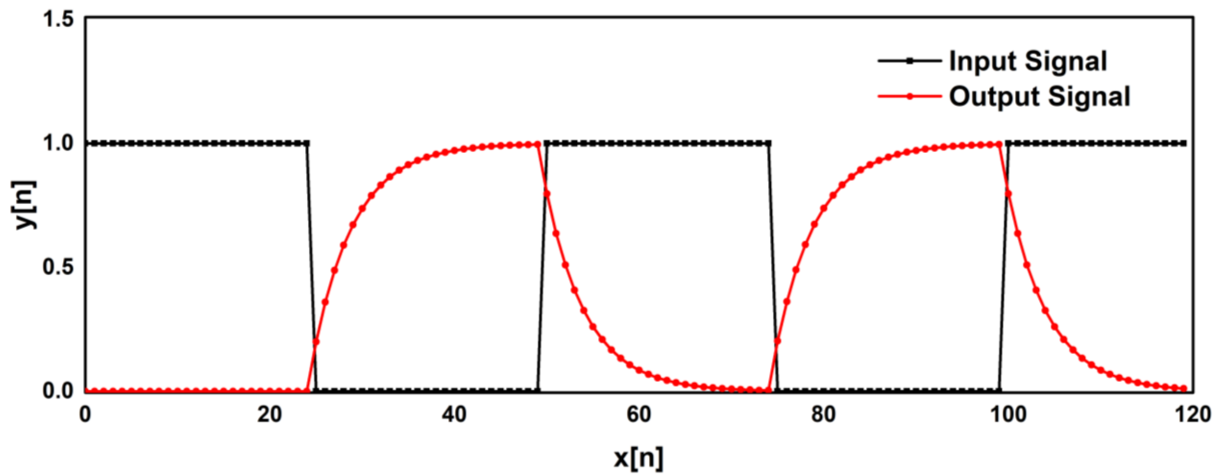


Figure 2.4: Output signal of leaky integrator with square input signal for *a* = 0.2, *g* = 0.2 and *τ* = 0.8.

A schematic of the integrator setup employing fiber-optic components and an optical integrator fabricated on SOI platform is shown in Figure 2.5. The loop includes an optical integrator fabricated on a SOI wafer, a semiconductor optical amplifier (SOA), an optical isolator (OI) and a band-pass filter (BPF). Two optical couplers (OC) with coupling ratio (*k*) of 0.5 are included in the SiPh based device as a form of directional coupler (DC) or Y–branch. Each port of integrator consists of a grating coupler designed for the center wavelength of 1552.1 nm, which is an average value of two operating wavelengths, 1553.3 nm for the input signal and 1551.0 nm for the circulating signal. OC_1 will act to couple the input signal into the loop, and OC_2 will be used to

extract the circulating signal out of the loop, leading to a photo-detector that converts an optical signal to an electrical signal. This converted signal is measured by oscilloscope as an output signal of the optical integrator. The behavior of the hybrid optical integrator can be described as follows.

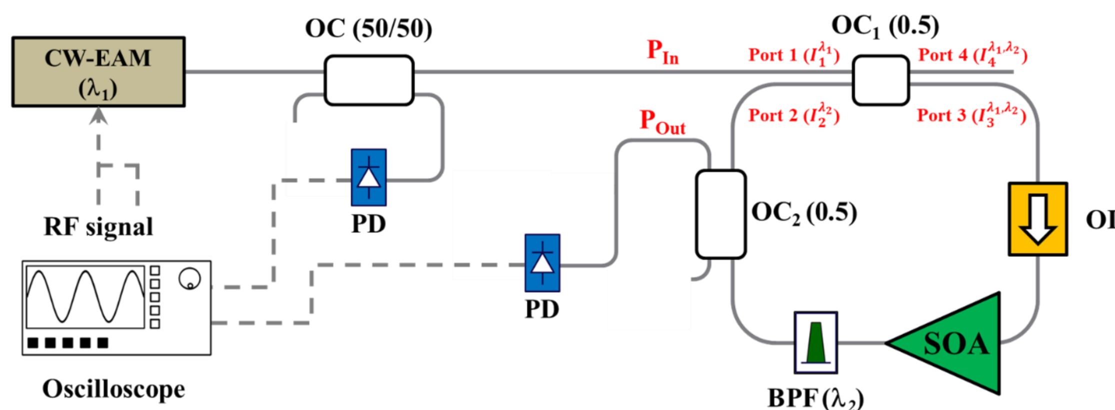


Figure 2.5: Schematic diagram of optical leaky integrator and experiment apparatus: The loop consists of two optical couplers (OC_1 and OC_2), semiconductor optical amplifier (SOA), optical isolator (OI), and band-pass filter (BPF).

The optical band-pass filter defines the resonance wavelength of the loop at λ_2 (integration wavelength, 1551.0 nm), which is different from the input wavelength λ_1 (1553.3 nm) in order to avoid the interference effects at OC_1 where circulating signal and input signal converge. The cross-gain modulation (XGM) effect in the SOA allows wavelength conversion from λ_1 to λ_2, and the BPF selectively passes through specific wavelength, λ_2, in the loop [11], [12]. In this integrator, the SOA is operated in the non-linear gain region, where the power of input signal modifies the gain of the SOA to be higher for low input powers and lower for high input powers. The integrated circulating signal at λ_2 increases when the gain exceeds the loss in the loop with low input signal power, or decreases otherwise.

The performance and operation principle of the leaky integrator can be described as follows. As mentioned previously, the gain in the SOA changes according to the input signal power. The modulated analog input signal first established the gain in the SOA and progressively modified by the re-circulating power in every roundtrip. Due to the inverse proportionality of the SOA gain via the input power, the gain and power of the output signal are high when the initial power of the input signal is low. Since the initial input power changes to a high value, a large number of carriers are occupied in the active region of the SOA, eventually the gain of the SOA for the re-circulating signal at wavelength λ_2 decreases and results in an overall gain that is lower than the loop-loss. As a result, the power of the signal that goes through a loop decreases in every roundtrip. Hence the gain of the SOA is a function of the intensity at port 3, which is inversely proportional to the gain for the re-circulating signal increases in every roundtrip, thereby reducing the rate of power declined in the output signal.

On the contrary, if the initial condition of the integrator is assumed to be at the high power of the input signal, low gain and low power output signal will take place. Due to low input power, there is an increase in the number of free carriers in the active region of the SOA, thus amplifying the re-circulating signal and exceeding the loss in the loop. This phenomenon leads to an increase in signal power while the SOA's gain decreases in every roundtrip. As a result, the rate of power increment in the output signal is reduced. Notice that the input signal at wavelength λ_2 does not circulate in the loop because the optical band-pass filter eliminates it. Therefore, the output signal of the integrator only contains the optical carrier component at wavelength λ_2 and can be extracted through OC_2. It is also possible to acquire the re-circulating signal at λ_2 through proper filtering at port 4 of OC_1.

Since the integrator operates with two optical signals at different wavelengths, its mathematical modeling can be done by using the modulus square of the complex field values. Let the modulated input signal in port 1 of OC_1, at wavelength λ_1 be denoted by $I_1^{\lambda_1}$, and the delayed output signal at wavelength λ_2 in port 2 by $I_2^{\lambda_2}$. Intensities of the signal at ports 3 and 4 are indicated by $I_3^{\lambda_{1,2}}$ and $I_4^{\lambda_{1,2}}$, respectively. The optical coupler, OC_1, and OC_2 have coupling intensity coefficients K_1 and K_2, the gain of SOA G, which is a function of intensity at port 3 $I_3^{\lambda_{1,2}}$, and the α indicates the sum of loss occurred by the loop including insertion loss at the grating coupler, loss in the optical filter, optical isolator, and propagation loss in the fiber, Si waveguide and optical coupler. The sampling period of the integrator T, which is the delay introduced by the loop defines the maximum operation frequency (or maximum frequency of the modulated input signal) of the integrator. The sampling frequency or free spectral range (FSR) for the loop can be described as

$$\mathrm{FSR} = 1/\mathrm{T} = c/(n_{eff}L) \tag{2.7}$$

where c is the speed of light in vacuum, n_{eff} is the effective refractive index of the waveguide, and L is the length of the loop [2]. The model parameters that define the performance of the integrator are based on the characteristics of the optical components and designed SiPh components. The operation of the hybrid optical integrator can be described as following the set of discrete equations:

$$I_3^{\lambda_{1,2}} = K_1 I_1^{\lambda_1}[n] + (1 - K_1) I_2^{\lambda_2}[n-1] \tag{2.8}$$

$$G[n] = A - B I_3^{\lambda_{1,2}}[n] \tag{2.9}$$

$$I_2^{\lambda_2} = C\alpha(1 - K_1)(1 - K_2)G[n] \tag{2.10}$$

where A, B, and C are real constants and sampling period T determines the interval between samples. For the simplicity of the mathematical model and performance description, a negative-slope linear approximation for the gain function in Eq. (2.9) is applied to define G. If SOA is not operating in the saturation gain region, this assumption cannot be used. As shown in Eq. (2.10), the intensity in port 2 $I_2^{\lambda_2}$ is directly proportional to the SOA's gain G due to an elimination of signal at wavelength λ_1. $I_2^{\lambda_2}$, which is proportional to the output signal intensity extracted from OC_2, can be expressed in terms of $I_2^{\lambda_2}$ and $I_1^{\lambda_1}$ by combining Eqs. (2.8) to (2.10).

$$I_2^{\lambda_2} = a + \tau I_2^{\lambda_2}[n-1] - g I_1^{\lambda_1}[n] \tag{2.11}$$

where $a = AC\alpha(1-K_1)(1-K_2)$, $\tau = -BC\alpha(1-K_1)(1-K_2)$, and $g = BC\alpha K_1(1-K_1)(1-K_2)$. Eq. (2.11) has identical functionality to Eq. (2.4), consists of similar terms and constant coefficient. Consequently, the proposed integrator can be considered as an inverted leaky integrator where the gain of the SOA, loss in the loop, and the coupling ratio of the optical coupler can be used to characterize its performance. In this thesis, the optical couplers are designed as a form of directional coupler and Y–branches, with the coupling coefficient of 0.5 for both OC_1 and OC_2.

2.3 Modeling and Simulation of Optical Integrator

The theoretical model introduced in Section 2.3 is simulated by MATLAB programming code to verify the operation of the hybrid optical integrator. All parameters used in the code are based on the simulation result from the Lumerical software, and measurements of components. In addition, propagation loss in the waveguide (3 dB/cm) with an additional loss such that sidewall roughness and fiber-to-grating coupler alignment error during the experiment (max. 1 dB per grating coupler)

are assumed and considered [3], [15]–[17]. Based on Eqs. (2.8) to (2.11), the theoretical performance of the hybrid optical integrator has been investigated, and the predicted outcome has been calculated. A delay block is introduced to represent the time delay created by the loop length. This time delay, T can be described as a function of the length of loop L, the effective refractive index of waveguide n_{eff}, and speed of light in vacuum c.

$$T = \frac{n_{eff}L}{c} \tag{2.12}$$

Figure 2.6(a) shows the simulation result of the hybrid optical integrator with the square-shaped input signal at 4 GHz. The optical input power for the simulation is setup as P_{in} = 3.1 dBm with maximum laser driving current of I_{in} = 150 mA. As discussed in theory, the intensities of light $I_2^{\lambda_2}$, $I_3^{\lambda_{1,2}}$, and $I_4^{\lambda_{1,2}}$ change at every circulation with the time delay introduced by loop length. Consequently, small discrete steps with the duration of each discrete step T, which is the delay time, can be observed from the output signal of the hybrid optical integrator.

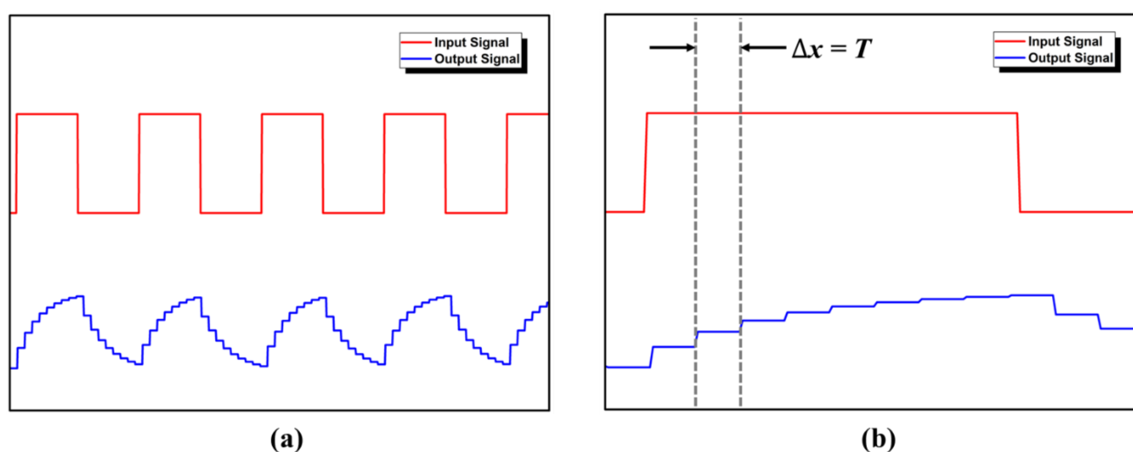


Figure 2.6: (a) Simulation result of the proposed optical integrator with a square-shaped input signal (red) and its output signal (blue) and (b) magnified image of (a).

The output format of the leaky integrator can be obtained by forming the envelope of each discrete step. According to Eq. (2.11), it is intuitive that the duration of each discrete step can be controlled by modifying the length of the loop L and effective index n_{eff}. In this investigation, the value of n_{eff} is fixed as approximately 1.5 for fiber and 2.4 for silicon waveguide on SiO_2. The length of the loop can be adjusted depending on the device design and fiber length. If the L is decreased, the delay time T eventually becomes smaller, thus providing enough steps to form a well-shaped envelope. In addition, due to large n_{eff} and a significantly shorter loop length of the Si waveguide, the hybrid optical integrator to operate at an input signal with a higher frequency. The SiPh based hybrid optical integrator has total loop length of Si waveguide approximately 2.75 mm and 5 m fiber cable, leading the delay time T as approximately 25 ns. Assume that a good shape of envelope output consists of 10 steps for the rising and 10 steps for the falling period. The hybrid optical integrator can process and obtain a high-quality output signal from the input signal frequency up to 2 MHz ($\cong$ 1 / (25 ns × 20)) [18]. Depending on the arrangement of the waveguide, grating couplers, direction couplers, and Y-branches, the optical loop length can be reduced, realizing signal processing at the range of Giga-Hertz throughout the Si waveguide. The SOA's gain G and the time constant τ can be easily modified by controlling the driving current of the SOA [14]. Proper value of initial gain G is obtained by simulation and modified by the experimental result.

2.4 Silicon Photonics Integrator Model

For decades, researchers aimed to find a way to control light and use it for the transmission and processing of information, an area of study known as Photonics [20]. The goal of researchers

studying photonics was to deliver an analog of an integrated electronic chip that could perform all of the required computational processes using photons while being space and time efficient. Scientists termed this technology photonic integrated circuit (PIC), devices that could integrate different optical components on a single substrate [21]. More recently, scientists were able to viably manufacture nanostructure devices and control the flow of light, due to the extensive development of technologies such as photolithography, molecular beam epitaxy (MBE), and chemical vapor deposition (CVD). In this study, the design of an optical integrator is done based on E-beam lithography fabrication. The device couples the light source from fiber to a grating coupler, delivering the signal to a Si waveguide and re-directing it to the fiber for the output signal measurement. The grating coupler, directional coupler, Y-branches, and waveguide devices are designed and simulated using Lumerical software. The detail of the simulation modeling of Lumerical is provided in Appendix. A.

2.4.1 Waveguide

A waveguide is a basic structure that provides the passage of an optical source in a silicon photonics device. The waveguide can deliver optical information through multiple components, linking different components on the substrate as an electronic wire or a fiber cable [3]. Under the consideration of choosing materials for the waveguide, silica was selected, as it is more readily available than any other material. The silica on silicon (SiO_2 – Si) or silicon on insulator (SOI) shows relatively high refractive index where the silicon (high refractive index of ~3.5) was embedded within silica (lower refractive index of ~1.4) [21]. In addition, the fabrication techniques for silicon are well established (courtesy of the microelectronic manufacturing), and the silicon is

compatible with other CMOS process. In this study, the proposed device is fabricated on an SOI wafer, where the established fabrication method can be fully utilized. The waveguide and other parts of the device are then designed based on the SOI wafer, where the silicon layer is a device layer on top of the SiO_2 layer (also called buried oxide layer or BOX layer).

The waveguide we utilize in this study is a strip waveguide, also known as a channel or photonic wire. The waveguide of the device is designed for a single transverse electric (TE) waveguide mode propagation, to prevent any interference and noise from different propagation speeds and the polarization of multi-mode [22]. Modes are the fields that maintain the same transverse distribution and polarization in all directions along the waveguide axis. TE mode is a waveguide mode where the electrical vector is always perpendicular to the direction of the propagation. Fundamental TE mode is a mode that has the lowest cut-off spatial frequency among multiple TE mode.

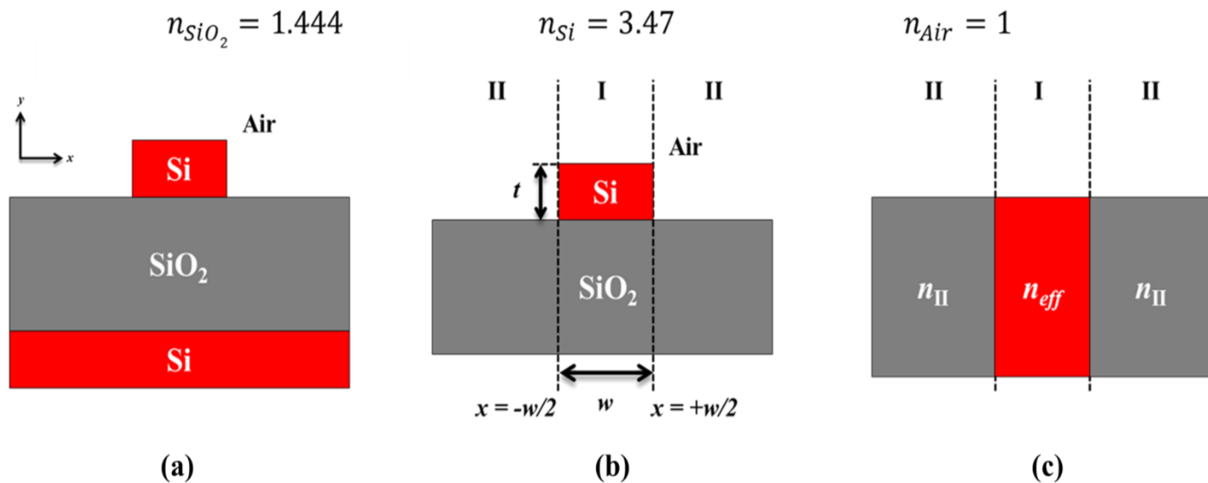


Figure 2.7: Schematic diagram of the Effective Index Method (EIM).

Before proceeding further into the design process, the base structure of waveguide is defined as shown in Figure 2.7(a). There are no other layers on top of the silicon layer as a form of cladding, due to the difficulty of developing uniform oxide cladding on top of a fabricated photonics device by E-beam lithography, especially for the grating coupler. With this structure, the cladding of waveguide is composed of air with the refractive index of $n_{air} \approx 1$. For the waveguide design, the one-dimensional calculation was first performed to determine the slab waveguide modes that only support single TE mode. The thickness of the waveguide is assumed to be 220 nm. Using Matlab code listed in Appendix D, the width waveguide width is found to be 500 nm. For the two-dimensional field profile, the effective index mode (EIM) is implemented [22], [23]. The basic idea of this method is to replace a two-dimensional waveguide with a one-dimensional one with an effective index derived from the geometry and refractive index. The structure of strip waveguide is shown in Figure 2.7(a), with the refractive indices of SiO_2 (n_{SiO_2} = 1.444), Si (n_{Si} = 3.47) and air (n_{air} = 1) at a wavelength of 1550 nm. EIM solves the mode condition in one-dimension for a certain mode and find the wave vector (or propagation constant). The effective index of a waveguide can be calculated in the following order. First, divide the structure into three regions as shown in Figure 2.7(b). Then, solve the mode condition for TE mode in the *y*-direction of a strip waveguide in Region I with Eq. (2.13) – (16) [22]:

$$ht = m\pi + \tan^{-1}\left(\frac{q}{h}\right) + \tan^{-1}\left(\frac{p}{h}\right) \tag{2.13}$$

$$h = \sqrt{k_0^2 n_2^2 - \beta^2} \tag{2.14}$$

$$p = \sqrt{\beta^2 - k_0^2 n_3^2} \tag{2.15}$$

$$q = \sqrt{\beta^2 - k_0^2 n_1^2} \tag{2.16}$$

where m is the mode order, n_1, n_2, and n_3 are the refractive indices of air, Si and SiO_2, respectively. β is the propagation constant of the mode confined in the waveguide, which is defined as $k_0 \cdot n_{effI}$ where n_{effI} is the effective index of the mode within the waveguide in Region I. Using EIM, the fundamental TE mode is confined in the strip waveguide with a dimension of 220 × 500 nm. From the Lumerical simulation, it can be observed that the waveguide is appropriate for the fundamental TE mode propagation (Figure 2.8).

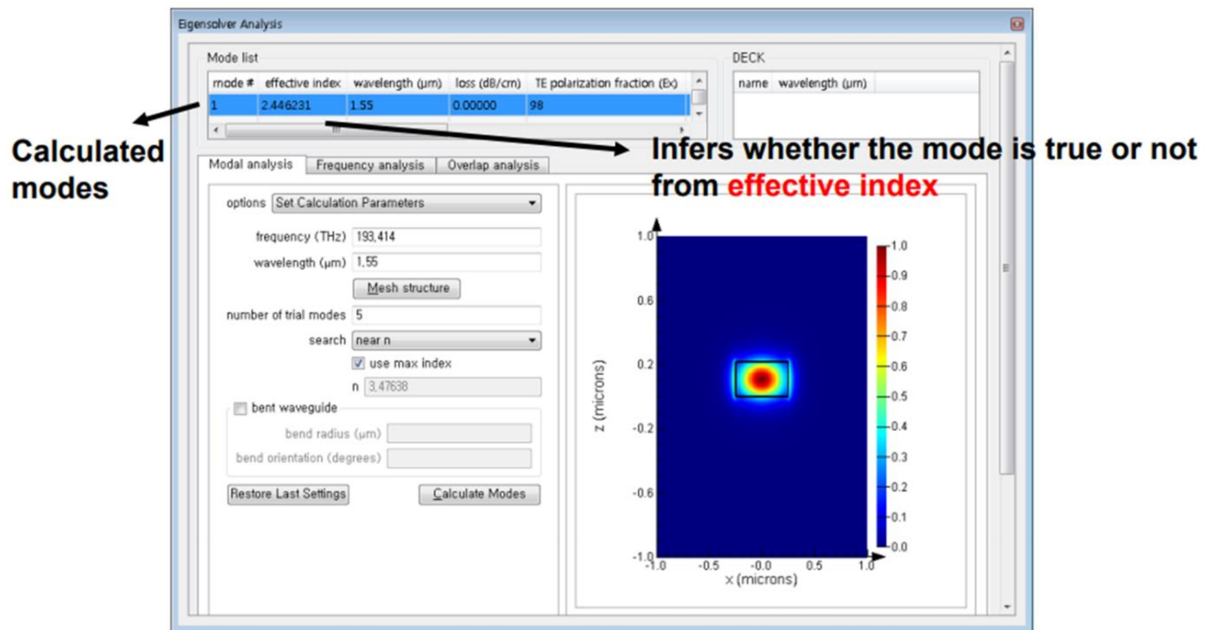


Figure 2.8: Two-dimensional field profile of TE fundamental mode in the waveguide.

Because we are not interested in the TM (Transverse Magnetic) mode, solving the mode condition in the x-direction is unnecessary. For the calculation of the TM mode, assumed that the structure is one-dimensional as shown in Figure 2.7(c), where the center region has a refractive index of n_{effI}. Now solve the mode condition in the x-direction with Eqs. (2.17) – (19) [22].

$$ht = m\pi + \tan^{-1}(\frac{\bar{q}}{h}) + \tan^{-1}(\frac{\bar{p}}{h}) \tag{2.17}$$

$$\bar{p} = \frac{n_2^2}{n_3^2} \cdot p \tag{2.18}$$

$$\bar{q} = \frac{n_2^2}{n_1^2} \cdot q \tag{2.19}$$

2.4.2 Grating Coupler

From Section 2.4.1, the fundamental TE mode is highly confined within the waveguide with dimensions on the order of a few hundred nanometers (220 × 500 nm). The nanoscale dimension provides a benefit for large-scale integration. However, the feature size of the waveguide leads to a problem of a large mode mismatch between optical fibers and the waveguide. The cross-sectional area of an optical fiber core (diameter of 9 μm) is approximately 600 times larger than that of the waveguide. Several approaches (edge coupling, surface plasmon coupling, *etc*.) have been conducted to solve the problem. One of the solutions found was the grating coupler, which provides better alignment process, no post-process after fabrication, flexibility in the design, and better coupling efficiency [24]. As so, we choose the grating coupler for the input/output (I/O) coupling techniques. In this section, the theoretical modeling of the grating coupler for a specific wavelength and the simulation process will be described.

A grating coupler is a periodic structure that can diffract light from the propagation in the waveguide to the free-space or the free-space to the waveguide [3]. The grating coupler is used as an I/O device to couple light between the fibers and the waveguide. Figure 2.9 shows the cross-section of a shallow-etched grating coupler design in an SOI wafer and critical design parameters

in one-dimension. The period of the grating is Λ (nm), the width of the grating teeth (nm) is w, *ff* is the duty ratio which is defined as $ff = w/\Lambda$, *ed* is the etch depth, and θ is the angle between the surface normal and the propagation direction of diffracted light. The thickness of the Si layer is 220 nm, while the BOX layer is 1 μm. As mentioned previously, there is no additional cladding layer. For this application, the cladding is air. The design of grating coupler requires the understanding of two fundamental theories; Bragg's law [25] which is applied to the periodic structures, and Effective Index Method (EIM) used to obtain the effective index of refraction of a slab waveguide. Based on the two theoretical approaches, the design parameters of the grating coupler will be determined and optimized by Finite-Difference Time Domain (FDTD) method in Lumerical.

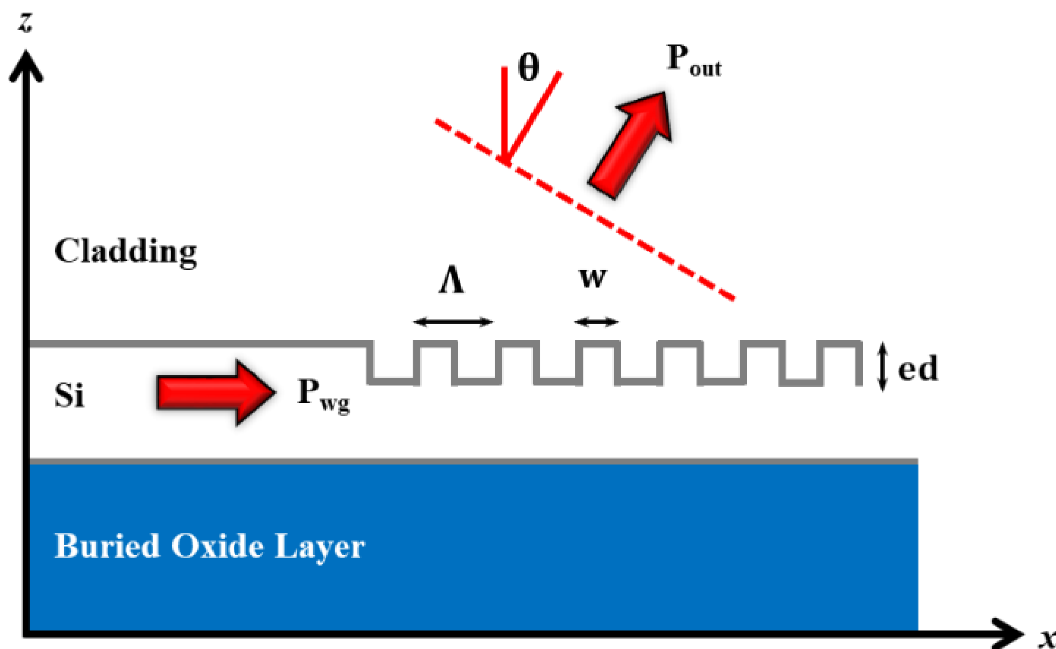


Figure 2.9: Schematic diagram of the cross-section of a grating coupler with the description of design parameters.

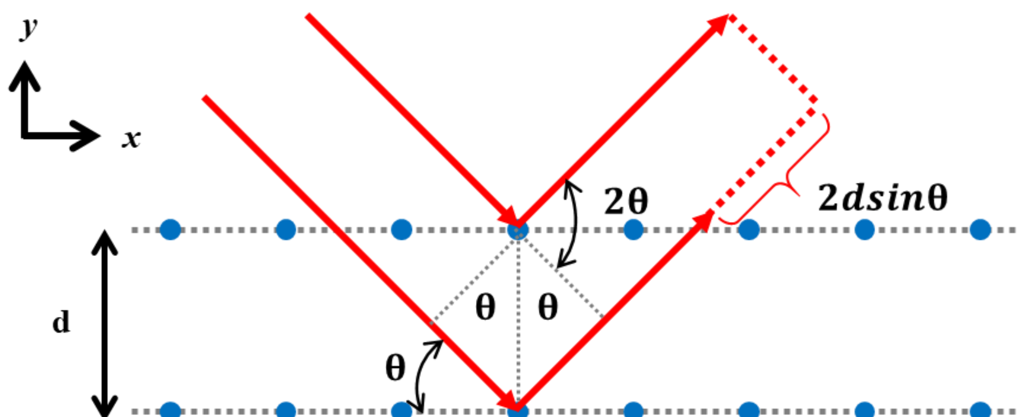


Figure 2.10: Schematic diagram of Bragg's Law.

Figure 2.10 shows the schematic diagram of Bragg's law. In the air, periodic dots are seperated by a distance of d in the y-direction. A plane wave is incident on the periodic structure and scattered by each lattice plane. Compared to the two planes in the y-direction, the diffracted plane waves by the lower lattice plane propagates an extra length of $2d\sin\theta$ than that of the top plane of dots. Depending on the phase condition, the interference occurs, and where the path difference is integer multiple of the wavelength, constructive interference occurs (Eq. (2.13)).

$$2d\sin\theta = m\lambda \tag{2.13}$$

The grating coupler discussed is a one-dimensional periodic structure, which can be described by Bragg's Law and Bragg Condition. Assume that the wave incident on a grating coupler is propagating in a slab waveguide and normal to the grating. In this case, the wave vector β can be expressed as

$$\beta = \frac{2\pi n_{eff}}{\lambda_0} \tag{2.14}$$

where λ_0 is the wavelength of the incident light source and n_{eff} is the effective index of the waveguide. For the first-order diffraction gratings (Figure 2.11), the Bragg condition can be written as

$$\beta - k_x = m \cdot K \tag{2.15}$$

where K denotes periodicity of the grating ($K = 2\pi/\Lambda$), m is the order of diffraction gratings, k_x is wave vector of the diffracted wave in the x-direction (length of the green arrow in the x-direction in Figure 2.11). The diffracted wave vector is traveling in the air ($n_{air} = 1$), so the wave vector of the diffracted wave can be written as

$$k = \frac{2\pi}{\lambda} \tag{2.16}$$

The diffraction angle of the wave can be described with k and k_x

$$\sin\theta = \frac{k_x}{k} = n_{eff}\frac{\lambda}{\Lambda} \tag{2.17}$$

Combining the Eq. 2.14, 2.16, and 2.17 into 2.15 simplifies the Bragg condition as

$$n_{eff} - \sin\theta = \frac{\lambda}{\Lambda} \tag{2.18}$$

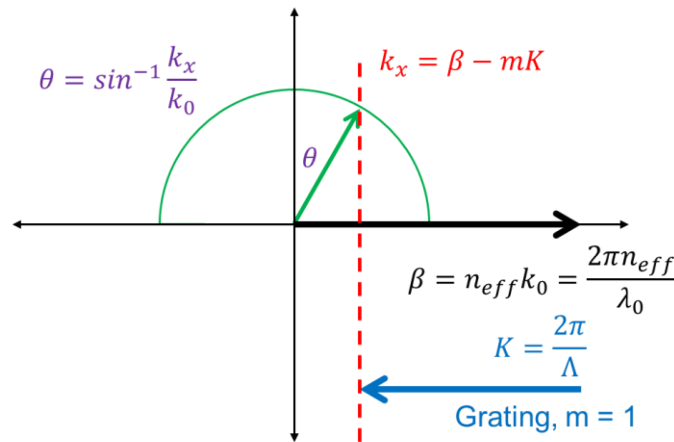


Figure 2.11: Schematic diagram of the Bragg condition for the grating coupler, where a black arrow indicates an incident wave and a green arrow indicates a diffracted wave.

Based on the Bragg condition, the design parameters of the grating coupler are calculated. Using the EIM, the effective index of the two silicon thickness can be obtained, assuming that the grating has an infinite width. Denote the n_{eff1} as higher thickness and n_{eff2} as the lower thickness at the periodic structure, the effective index of the grating region can be written as

$$n_{eff} = ff \cdot n_{eff1} + (1 - ff) \cdot n_{eff2} \tag{2.19}$$

Assume that the 220 nm slab waveguide with 70 nm shallow etched grating, leads to a grating with a refractive indices n_{eff1} = 2.848 and n_{eff2} = 2.534 at the wavelength of 1550 nm. From Eq. 2.20, the grating period can be calculated as

$$\Lambda = \frac{\lambda}{n_{eff} - sin\theta} \tag{2.20}$$

If the initial design has 50% fill factor (*ff*), an incident angle of 8° (θ), the grating period is approximately 607 nm. Based on this result, the optimization process is done using FDTD simulation in Lumerical.

Lumerical FDTD is used to design silicon photonics components to optimize the performance of the grating coupler and the directional coupler. The theoretically driven model is then verified, revised and optimized at the operation wavelength, with minimized insertion loss. Following the Appendix A, the simulation model is created as shown in Figure 2.12. Based on this model, simulation is done to optimize the design of the grating coupler to maximize the coupling of the light from the fiber to the grating coupler at the wavelength of 1550 nm. The minimum resolution of each parameter is 5 nm based on the fabrication resolution. Figure 2.13 shows the optimized design parameter of the grating coupler. The period of the grating is 610 nm, the width of grating teeth is 305 nm, the etch depth is 70 nm, and the incident angle is 8°. Coupling light from a grating

coupler to a fiber induces approximately -2.3 dB insertion loss. On the other hand, -3 dB insertion loss occurs from the coupling of light.

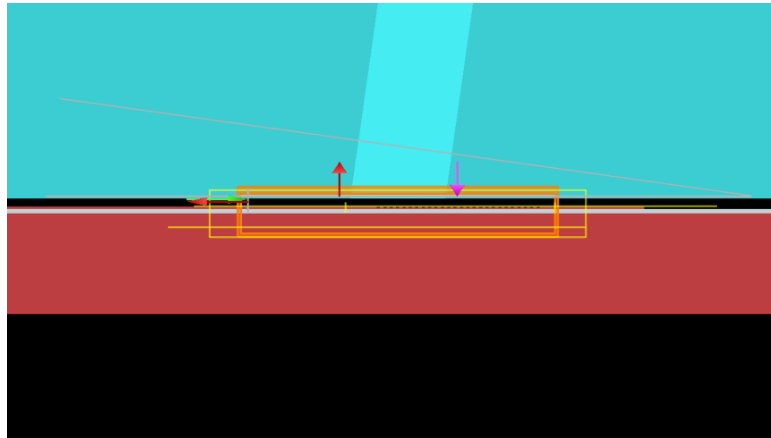


Figure 2.12: The final simulation model for the grating coupler.

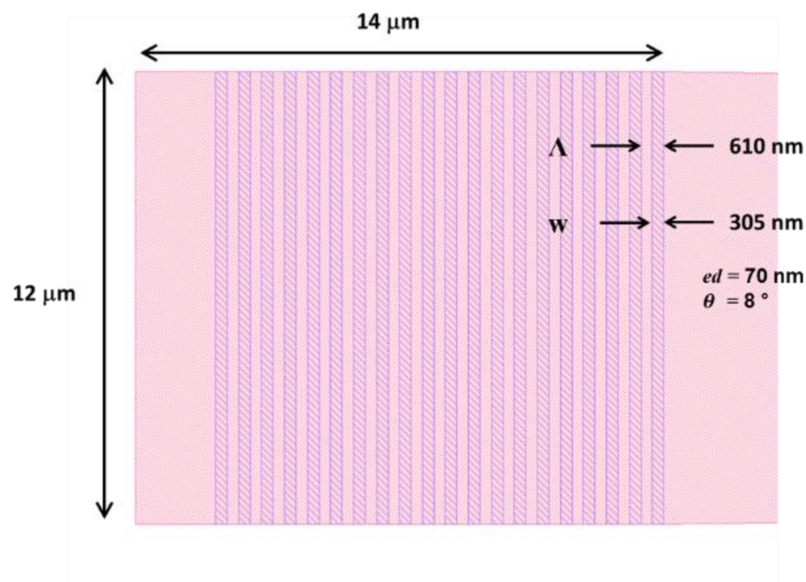


Figure 2.13: Optimized design of grating coupler at the wavelength of 1550 nm.

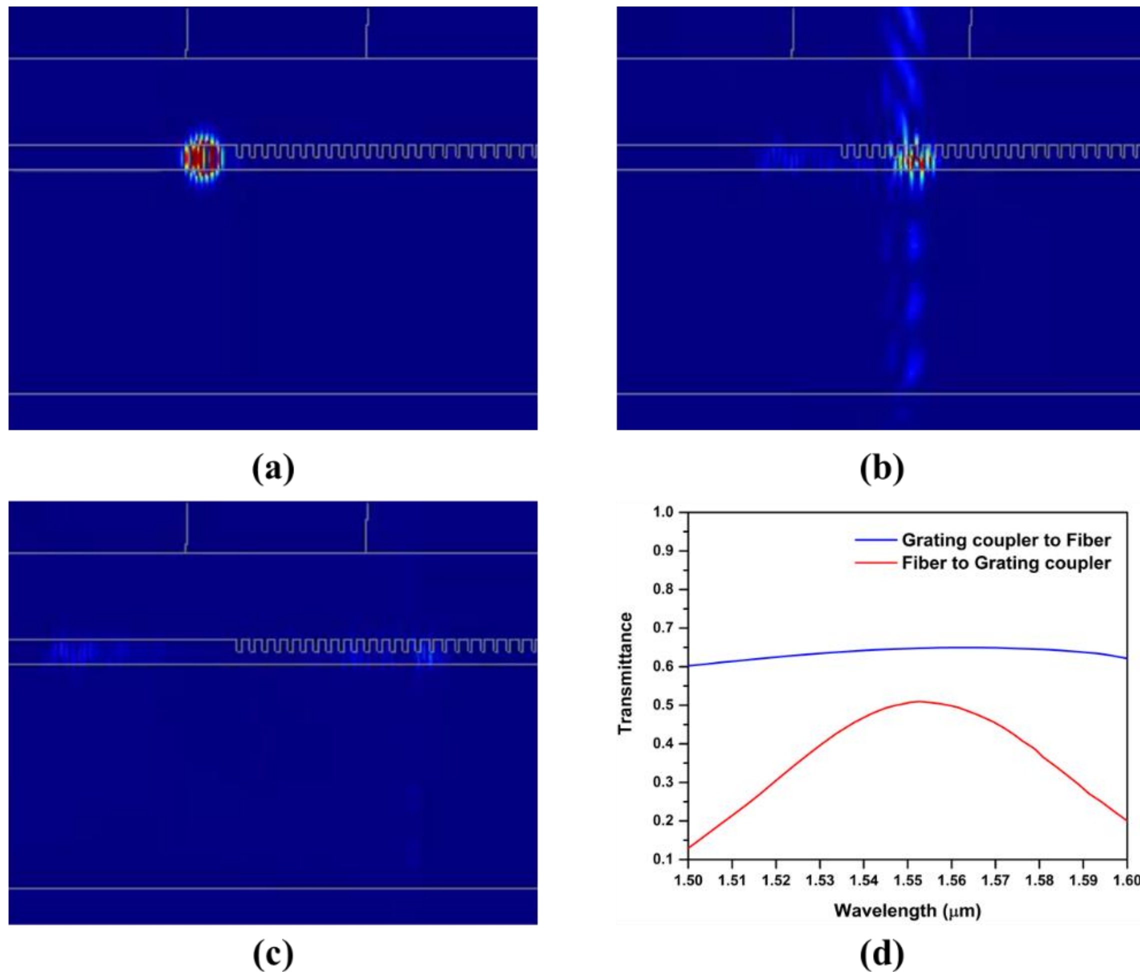


Figure 2.14: Simulation result for the grating coupler: (a) Light propagation from the waveguide to a grating coupler, (b) light coupling from grating coupler to optical fiber, (c) light propagation after coupling, and (d) transmittance of the grating coupler.

2.4.3 Directional Coupler

The directional coupler is widely used for photonics systems such as power splitter or combiner, micro-ring resonator, and Mach-Zehnder interferometer. Conventional directional coupler consists of two parallel waveguides that are very compact, and sensitive to the wavelength and polarization

of the light source. The directional coupler on SOI is designed to couple light through evanescent fields corresponding to the individual guided modes of two waveguides. The coupling coefficient of the directional coupler is controlled by the length of the coupling region and the spacing between the two waveguides. In this section, the design of the directional coupler based on the strip waveguide from theory to simulation will be demonstrated.

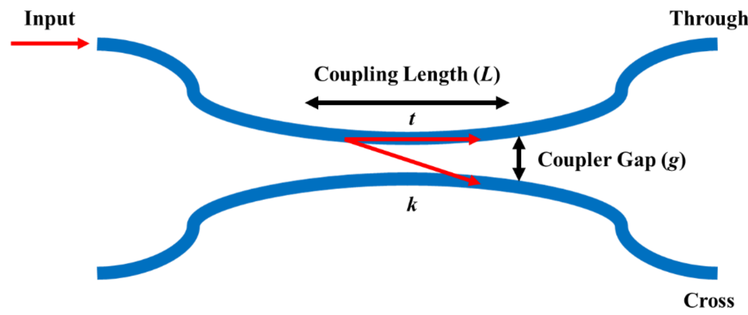


Figure 2.15: Schematic diagram of a directional coupler.

Figure 2.15 shows the schematic diagram of a directional coupler with essential design parameters, coupling length L, coupler gap g, and coupling coefficient κ and t. According to coupled mode theory [22], the power ratio coupled from one waveguide to the other can be expressed as

$$\kappa^2 = \frac{P_{cross}}{P_0} = \sin^2(CL) \tag{2.21}$$

$$t^2 = \frac{P_{through}}{P_0} = \cos^2(CL) \tag{2.22}$$

where P_0 is the input power, $P_{through}$ is the power to the through port, P_{cross} is the power coupled to the cross port, L is coupling length, and C is the coupling coefficient. Assuming there is no loss due to coupling and propagation through the directional coupler, the summation of the coupling coefficient can be expressed as

$$\kappa^2 + t^2 = 1 \tag{2.23}$$

From the 'supermode' analysis, denote n_1 and n_2 as the first two eigenmodes of the coupled waveguides (even and odd mode, respectively) [26], [27]. By applying the eigenmode expansion method, the coupling coefficient C can be found as

$$C = \pi\Delta n/\lambda \tag{2.24}$$

where $\Delta n = n_1 - n_2$. As two modes are propagating in the waveguide, the optical power oscillates back and forth between the two waveguides. The cross-over length L_x, where the minimum length required for the maximum optical power transfer from one waveguide to the other waveguide, occurs after the π phase shift difference between the modes (Eq. (2.25)).

$$L_x(\beta_1 - \beta_2) = \pi$$

$$L_x = \frac{\pi}{\beta_1 - \beta_2} = \frac{\lambda}{2\Delta n} = \frac{\lambda}{2(n_1 - n_2)} \tag{2.25}$$

According to Reference [28], the relationship between the coupler gap and coupling length can be found as Eq. (2.15). Using this equation and Eq. (2.21), the field coupling coefficient, κ, can be calculated as Eq. (2.27) for any coupler gap and length.

$$L_x = 10^{(0.0037645g + 0.799434)} \tag{2.26}$$

$$\kappa = \left(\frac{P_{cross}}{P_0}\right)^{1/2} = \left|\sin\left(\frac{\pi\Delta n}{\lambda}\right) \cdot L\right| \tag{2.27}$$

Based on the theory, a directional coupler with a coupling length of L_x = 37.5 µm and a coupler gap of g = 200 nm is obtained and optimized with Lumerical. The simulation model of the directional coupler is provided in Figure 2.16 and the simulation result is shown in Figure 2.18. From the simulation, the optimized coupling length is 50.8 µm with the coupler gap of 200 nm (see Figure 2.17). The light propagates from left to right, and approximately 20% of the input power of light is coupled to cross port, while 22.5% of light propagate to the through port. From

this result, the coupling ratio and coupling loss can be calculated as 47/53 and -3.27 dB, respectively.

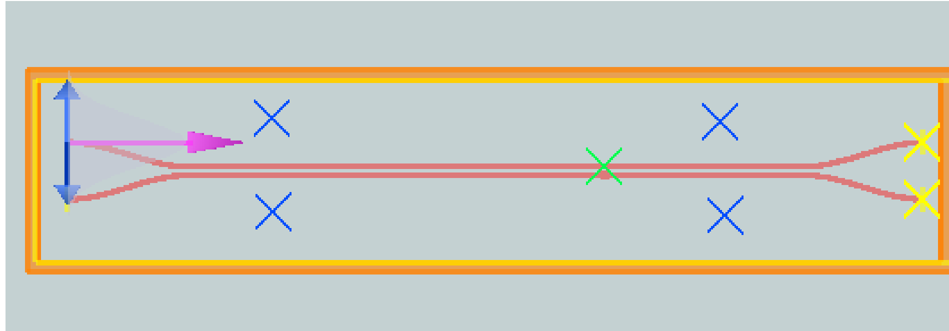


Figure 2.16: The simulation model of a directional coupler.

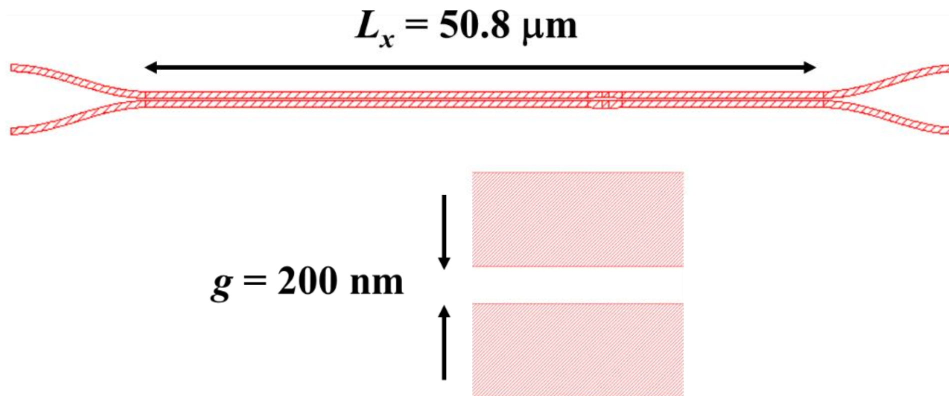
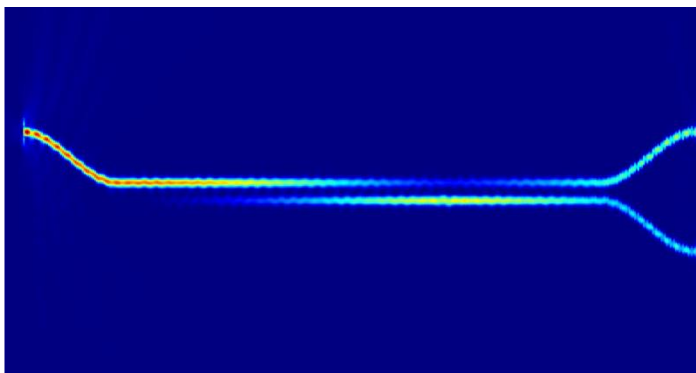
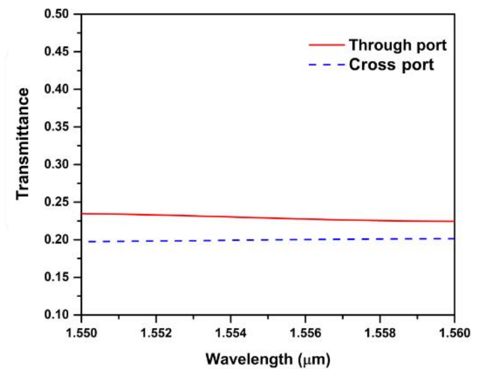


Figure 2.17: Optimized directional coupler design parameters.





(a) (b)

Figure 2.18: Simulation result of the optimized directional coupler.

3. FABRICATION AND EXPERIMENT

3.1 Fabrication of Optical Integrator on SOI Wafer

The SiPh devices were fabricated on the SOI wafer by E–Beam lithography. First, the layout of SiPh devices was done by K–Layout. Second, the SOI wafer thinning was done to obtain Si layer thickness of 220 nm to increase the yield rate of fabrication. Then the layout file and SOI wafer were sent to the University of Minnesota for the E–Beam lithography process.

3.1.1 K–layout for E–Beam Lithography

For the E–beam Lithography, a GDS file format of device layout is required. There are numerous physical mask layout tools available for electronics, MEMS, photonics and other applications [29] –[31]. Among them, K–layout is chosen due to easy access and integration with other photonics simulation software, especially with the 'Lumerical.' In order to enhance design efficiency and reliability, we used E-beam Package Design Kit (PDK) which is an open source design library made by Ref. Lukas Chrostowski and his team at University of British Columbia [32]. For the Layout software, K-Layout is selected. E-bema PDK offers basic structures, such as waveguides, a ring resonator, grating couplers, and so on, and a number of design examples. These libraries allow us not to make unexpected design errors. Details of the design procedure are given in the Appendix B. Following the instruction, the grating coupler and the directional coupler are successfully added to the library. One of the advantages of the installed package is that arrangement and routing of components become extremely simple. For example, a waveguide that connects grating couplers or directional couplers can be placed by using the function 'Path to Waveguide'

as shown in Figure 3.1. Creating waveguide proximity at the end of components and clicking ‘w’ leads to an accurate arrangement of the waveguide and the components automatically. From various functions provided by the package, the design procedure becomes concise and faster.

Figure 3.1: (a) ‘Path to Waveguide’ function, (b) misaligned waveguide and component and (c) perfectly fitted waveguide to a component by using ‘w’ function of the package without overlap.

After the essential components are added to the library, a 4-inch wafer size circle and 36 boxes with a dimension of 1 cm × 1 cm for the cells are drawn (Figure 3.2). Alignment marks are also included for the accurate alignment of the two-step etching process because the grating coupler includes shallow etching of 70 nm thickness to fabricate grating teeth. Then the nine devices, which have a specific purpose, are then placed into each box (Figure 3.3). Table 3.1. shows the experimental purpose of each device included on the SOI wafer. The K-layout file created in GDS file format is then verified by design rule check (DRC) and revised appropriately for the E-beam lithography software (Cygwin). The design file is then sent to the University of Minnesota with an SOI wafer for the E-beam lithography.

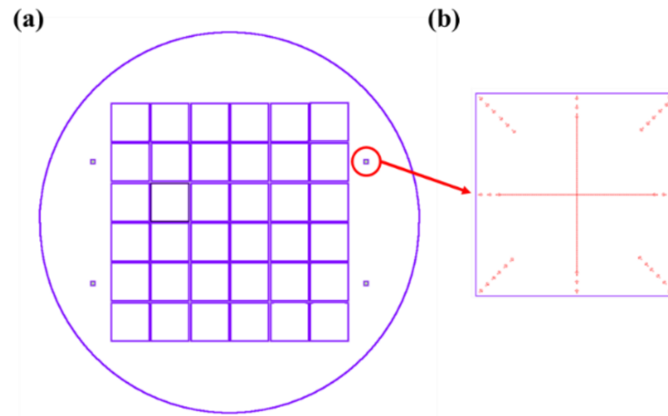


Figure 3.2: (a) Arrangement of cells on the 4-inch wafer and (b) alignment mark.

Table 3.1: Experiment objects of nine different devices.

Device		**Experiment Objective**
Figure 3.11	**(a)**	Propagation loss due to *waveguide length*
	(b)	Coupling ratio and loss of *directional coupler*
	(c)	Coupling ratio and loss of *Y-branches*
	(d)	Performance of proposed design using *fiber array*
	(e)	Performance of proposed design using *fiber array*
	(f)	Performance of proposed design using *4 fibers* (Optical path length of *4,000 µm approximately*)
	(g)	Performance of proposed design using *4 fibers* (Optical path length of *4,000 µm approximately*)
	(h)	Performance of proposed design using *4 fibers* (Optical path length of *10,600 µm approximately*)
	(i)	Performance of proposed design using *4 fibers* (Optical path length of *10,600 µm approximately*)

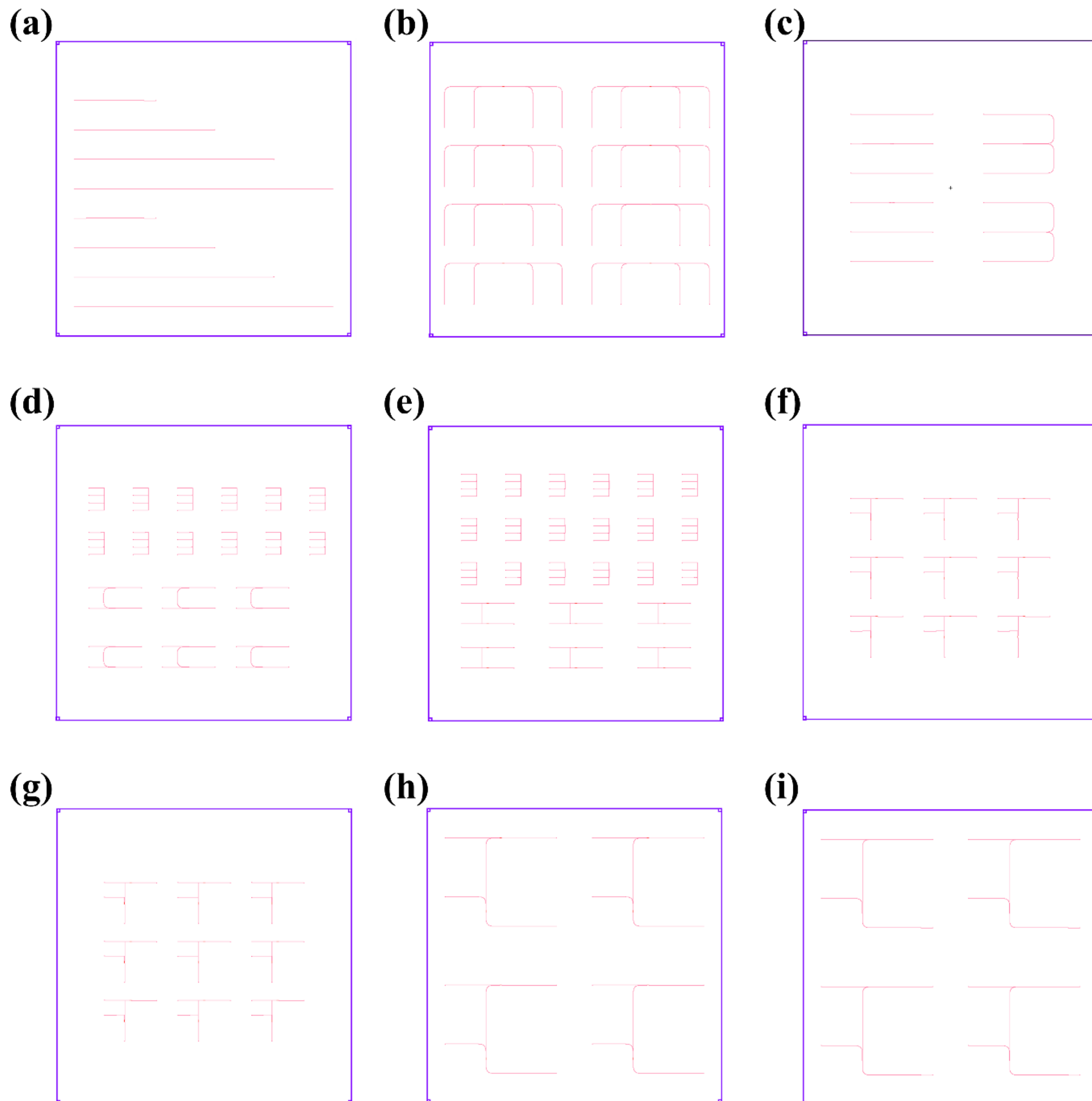


Figure 3.3: Nine different sets of devices for specific experimental purposes.

3.1.2 Wafer Thinning

The SOI wafer (S.E.H. America) we used was 2 µm thick device layer with ± 150 nm thickness variation, 1 µm buried oxide (BOX) layer with ± 80 nm thickness variation. The device layer is a

Si layer from which the structures are going to be fabricated. From trial and error, the defects and fabrication error is minimized when the thickness of the device layer is 220 nm ± 30 nm. In the case of 2 μm thickness of the device Si layer, disconnection of the waveguide and defects on the edge of the nanoscale structure were found, which reduces the yield rate. For the higher yield rate of E-beam lithography, the desired thickness of device layer is approximately 220 nm ± 30 nm, so the device layer must be thinned by multiple oxidations, and buffered oxide etch (BOE) process (Figure 3.4).

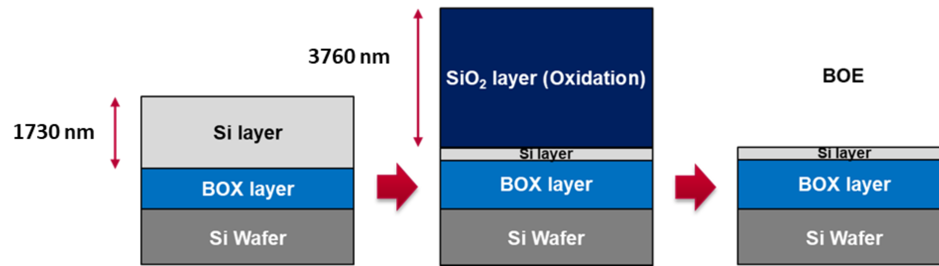


Figure 3.4: Schematic diagram of device layer thinning process by oxidation and BOE.

The Deal-Grove model (Eqs. (3.1) to (3.3)) describes the relationship between oxide thickness and oxidation time [33].

$$x_{ox} = \frac{A}{2}\left(-1 + \sqrt{\frac{4B}{A^2}(t+\tau) + 1}\right) \tag{3.1}$$

$$\tau = \frac{x_i^2}{B} + \frac{A}{B}x_i \tag{3.2}$$

$$x_{si} = 0.46x_{ox} \tag{3.3}$$

where t denotes the oxidation time, A and B are temperature dependent constant and τ is a parameter that affect the initial oxide thickness x_i. The parameter A and B are different for every

furnace, so from several oxidation of Si layer, A and B are first calculated to predict the desired time to oxidation thickness relations. Substitute Eq. (3.1) and (3.3) to (3.2) give Eq. (3.4),

$$\overbrace{\begin{bmatrix} x_{ox} - x_i & t \end{bmatrix}}^{X} \overbrace{\begin{bmatrix} A \\ -B \end{bmatrix}}^{Z} = \overbrace{-x_{ox}^2 + x_i^2}^{Y} \tag{3.4}$$

where x_i can be assumed to be 1 nm. By applying the pseudo inverse matrix method, Matrix Z can be estimated as shown in Eq. (3.5)

$$\mathrm{Z} = (X^T X)^{-1} X^T Y \tag{3.5}$$

The thickness of Si and SiO_2 layers are measured by thin film measurement equipment (Filmetric F20). This equipment provides only one spot thickness information. Figure 3.5 shows 73 points on the wafer that were used to create a contour map of thickness. From the multiple oxidations of the Si layer, the time and oxidation layer thickness data were collected (Table 3.2). Based on this data, A and B are calculated using Eq. (3. 5) as

A = 0.548 μm, B = 0.230 $\mu m^2/hr$

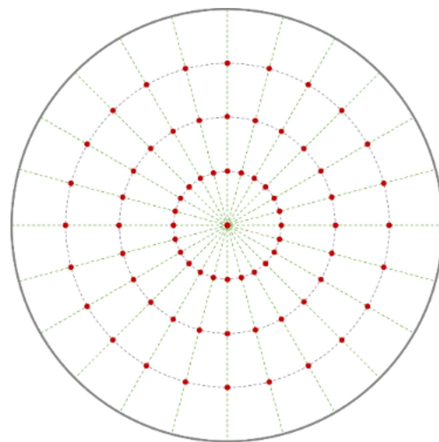


Figure 3.5: Thickness measurement spots for the thickness contour map.

Using the calculated numbers (A and B) for Eq. (3.1) and the SiO_2 thickness according to oxidation time, a plot (Figure 3.6) is formed. With the factors A and B, an R-squared of 0.9944 is achieved (1.0 represents no error between the fitted equation and experimental data). Based on this result, the Si thickness can be successfully etched with the desired thickness by manipulating oxidation time. Using an etch rate of BOE, 1.3 nm/s, the SiO_2 layer can be removed accurately. However, we need an oxidation layer thickness of 4 µm, which takes an enormous amount of time to oxidize at once. As so, the oxidation and etching process is done four times to accurately accomplish the etching process to the desired thickness of the device layer. During the multiple oxidation and etching processes, the roughness or variation of thickness on the device layer did not show significant changes. The final thickness contour map of the device layer is shown in Figure 3.8. Due to the significant variation of the initial wafer thickness (Figure 3.7), we decided to etch 1730 nm of the Si wafer, providing the largest area of 220 nm thickness of Si layer at the end of the thinning process. From preforming the etching and BOE process four times, the desired Si layer thickness can be achieved as shown in Figure 3.9. The red line in Figure 3.8(c) shows the thickness of the Si layer is approximately 220 nm.

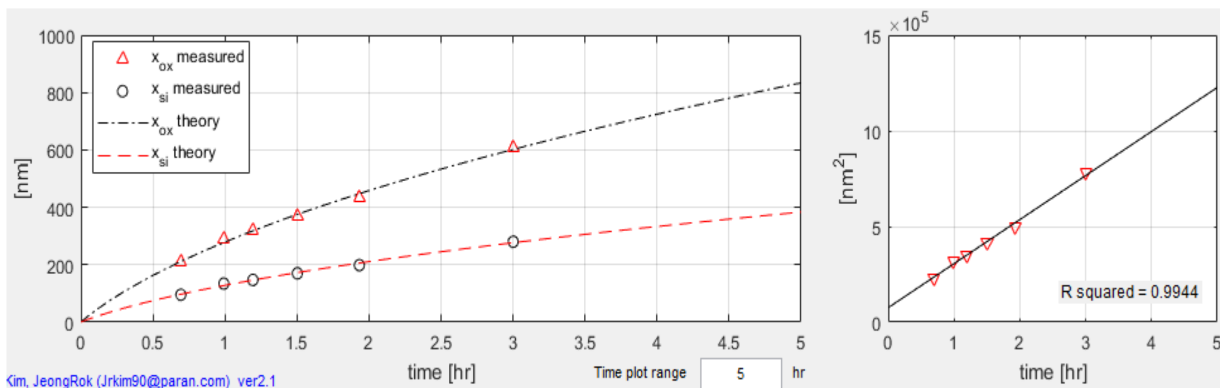


Figure 3.6: Deal-Groove curve and linear regression line for R-squared calculation.

Table 3.2: Experimental result of oxidation time versus SiO_2 thickness for Deal-Groove model.

t (hours)	x_{ox} (nm)	x_i (Native oxide, nm)
0.694	207.5	1
0.992	291.8	1
1.194	319.9	1
1.503	369.9	1
1.933	431.7	1
3.001	609.1	1

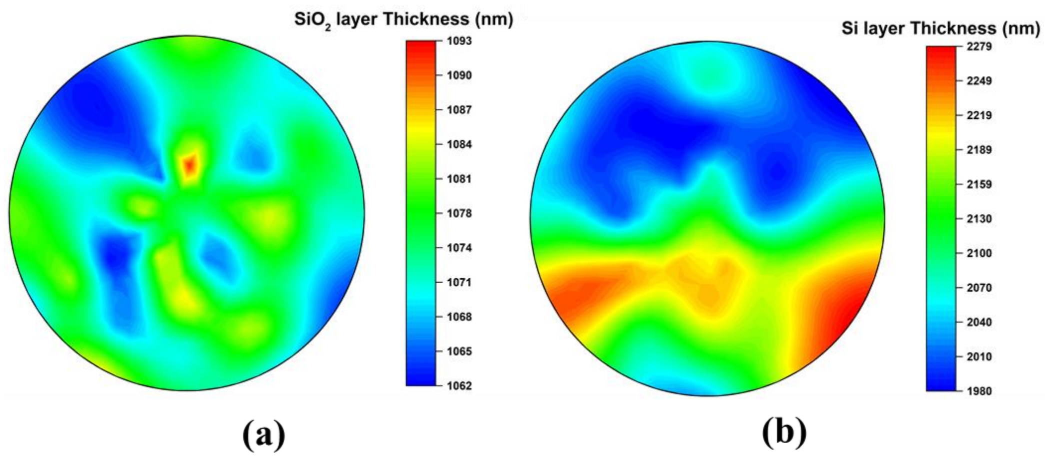


Figure 3.7: The initial thickness of SOI wafer: (a) SiO2 layer and (b) Si layer.

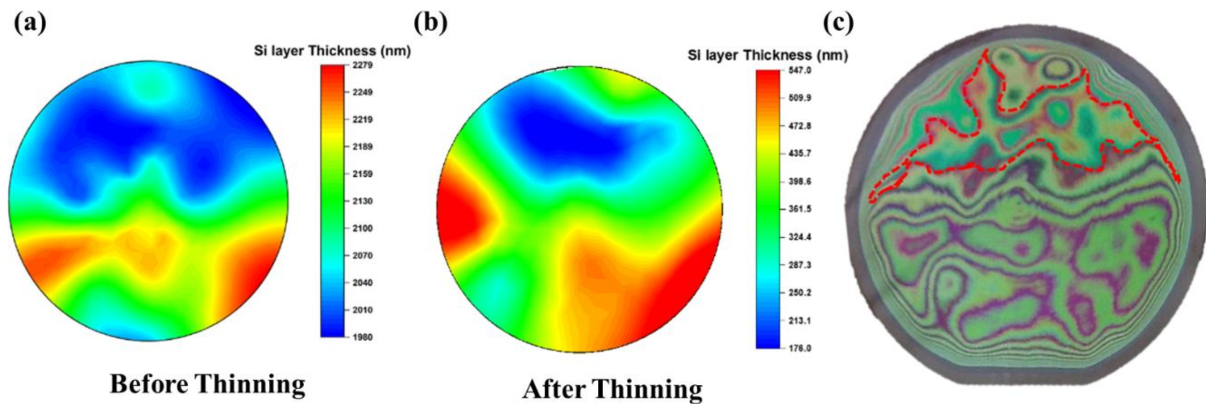


Figure 3.8: Contour map of Si layer thickness (a) before, (b) after thinning and (c) image of SOI wafer after thinning process.

3.1.3 E–Beam Lithography

The E-beam lithography was performed by engineers at the University of Minnesota. The wafer was rinsed with DI water for 3 minutes and dried with a nitrogen (N_2) gun. Prior to spin coating, the HSQ resist, a dehydration bake was performed on the wafer using a 180 °C hotplate for 4 minutes. Then, the wafer was allowed to cool for at least 1 minute, allowing it to come back down to room temperature. Next, the resist was spin coated. Spin coating of the ~8% HSQ resist (1 part Dow Corning's FOX-16 (16%) resist diluted with 1 part MIBK) was carried out at 5000 rpm for 30 seconds. to achieve a 200 nm film. Then the resist was soft-baked at 80 °C for 4 minutes on a hotplate. Patterning of the device waveguides was performed using a Vistec EBPG 5000+ e-beam lithography system. The relevant parameters for the fracturing of the design file were as follows: 1 nm fracture resolution, 10 nm beam step size and proximity effect correction. Exposure was performed using a 100 kV, 30 nA beam, with a base dosage of 1800 $\mu C/cm^2$. Development was carried out using a MF 319 Developer (2.3% TMAH based) for 3 minutes. Most of the wafer was

cleared in the first minute. However it took an additional 2 minutes to clear the optical input regions and spiral regions where the patterns were more dense, and thus halo features had formed around the intended features. Experience has shown one can go up to 4 minutes total if additional dense regions need to be cleared of their corresponding halos. The wafer was then rinsed with DI water for 3 minutes and dried with an N_2 gun. Etching of the top silicon layer waveguides (220 nm thick) was performed using a PlasmaTherm Deep Trench Etcher and a non-Bosch recipe developed at Cornell Science & Technology Facility for photonics applications; cnf-14-v [34]. The etch rate for this recipe was determined to be the following: 200 nm/minute for Si, 70 nm/min for soft-baked HSQ, and 35 nm/min for thermal oxide. Etching was performed for 95 seconds. to clear the 220 nm of silicon, which represents about a 20% over-etch, but this was necessary to account for any non-uniformities in the top silicon. Next, the HSQ resist was stripped by submerging the wafer in 10:1 buffered oxide etch (BOE) for 15 seconds, and then rinsing it in DI water for 3 minutes, and then drying it with a nitrogen gun. The wafer is then prepared for the second layer of patterning. The wafer was again given a dehydration bake on a hotplate at 180 °C for 4 minutes. After cooling, PMMA C2 resist was spin coated at 1000 rpm on the wafer to form a 200 nm thick layer of positive resist.

The second layer of patterning, which consisted solely of the corrugations for the optical input-output, had a minimum lateral spacing size of 305 nm and was later etched to a depth of 70 nm. The patterning was once again carried out using the Vistec EBPG system at an acceleration voltage of 100 kV and a 30 nA beam current. Development was carried out using immersion in a 3:1 IPA:MIBK solution for 30 seconds. Isopropanol alcohol (IPA) was used to rinse the wafer, and then it was dried using a nitrogen gun. Etching of the corrugations to a depth of 70 nm was again

carried out using a PlasmaTherm Deep Trench Etcher and the recipe cnf-14-v. The etch time to achieve a 70 nm depth was 21 seconds. The cnf-14-v etch recipe consists of six steps, but step 5 is considered the main etching step, and its process parameters are the following: C_4F_8 = 63 sccm, SF_6 = 27 sccm, Ar = 40 sccm, O_2 = 10 sccm, Pressure = 14 mTorr, RF_1 = 10 Watts, RF_2 = 700 watts, DC Bias = 85 Volts. After the etching of the corrugations, the PMMA resist was stripped for 15 minutes by immersion in NMP solvent that was heated to 60 °C on a hotplate. The wafer was then rinsed in acetone, methanol, and isopropanol and dried with a nitrogen gun.

3.2 Experimental Setup

In this section, the detailed experimental setup for the fiber-optics based experiment and light coupling setup for the SiPh device is described. The main focus of this section is the setup for the fiber array and its arrangement on top of grating coupler. There are two methods to couple the light source into the SiPh device, one is using fiber array, and the other is using four fiber probes. The fiber array unit is introduced to reduce the stress of alignment and increase the efficiency of experimental procedures. It also provides the advantage of reducing waveguide length compared to using fiber probes. Using four fiber probes requires extra space between probes with inevitable increase in the waveguide length. We used a fiber array of eight channels (Figure 3.9) which has more channels than our number of I/O units. For the alignment of fiber and grating coupler, custom parts were designed, and two cameras were adopted to observe the alignment procedure. The complete experimental setup will be discussed in Sections 3.2.1 and 3.2.2.

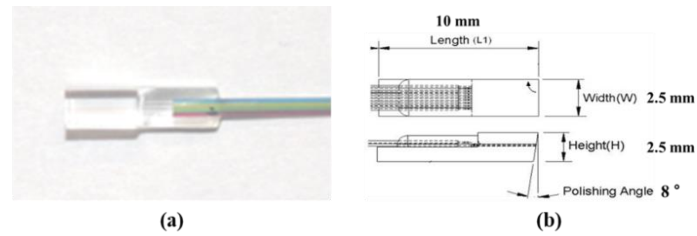


Figure 3.9: (a) Image of fiber array and (b) dimension of the fiber array.

3.2.1 Fiber-Optic Integrator

Based on the proposed model of the optical integrator in Section 2.2 and Figure 2.4, appropriate devices were selected and assembled in a system as shown in Figure 3.10. Prior to the experimental verification of the performance of the optical integrator, each device was separately tested to determine the insertion loss, peak wavelength, and gain characteristics which critically affect the operation of the system. The fiber-optic devices and the insertion loss are listed in Table 3.3.

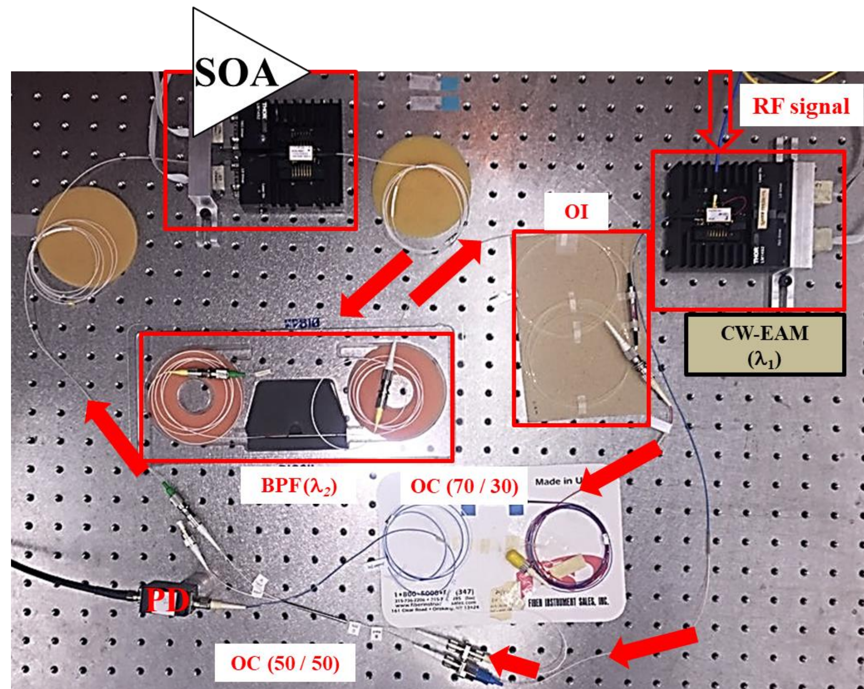


Figure 3.10: Experimental setup of fiber-optic integrator.

Table 3.3: List of equipment and insertion loss (if any occurs).

Name	Model	Insertion loss (dB)
Band-pass filter	–	1.087 at λ = 1551.00 40.00 at λ = 1553.95
CW-EAM	1905 LMI, AVANEX	–
Laser Diode	FLDF10NP, Thorlabs	–
Laser Diode Mount	LM14S2, Thorlabs	–
Laser Diode Controller	LDC-3900, ILX Lightwave	–
Optical Coupler (50/50)	–	3.556
Optical Coupler (70/30)	–	1.984 at 70 5.084 at 30
Optical Isolator	–	7.979 at λ = 1551.00 1.930 at λ = 1553.95
Optical Spectrum Analyzer	Agilent 86140B, Agilent	–
Oscilloscope	Agilent 54622D, Agilent	–
Photodetector	DET01CFC, Thorlabs	–
Semiconductor Optical Amplifier	SOA-5901, COVEGA	–
Signal Generator	Agilent 33120A, Agilent	–

3.2.2 Optical Integrator based on SOI platform

The schematics of the experimental setup for the SiPh device is shown in Figure 3.11. Two cameras, for the top view and the side view, were connected to the two monitors, and the input light source was connected to the fiber array or fiber probes. The SiPh die was placed on top of the *xyz* stage, which includes the nano-piezo stage to control nanoscale alignment between fiber and grating coupler (Figure 3.12). The fiber array and fiber probe were connected to the *xyz* stage and rotational stage that can control the incident angle and precise movement of fiber. To avoid vibration of apparatus while taking data, a vacuum plate that holds the SiPh die and the fiber array holder were designed and fabricated (see Figure 3.13).

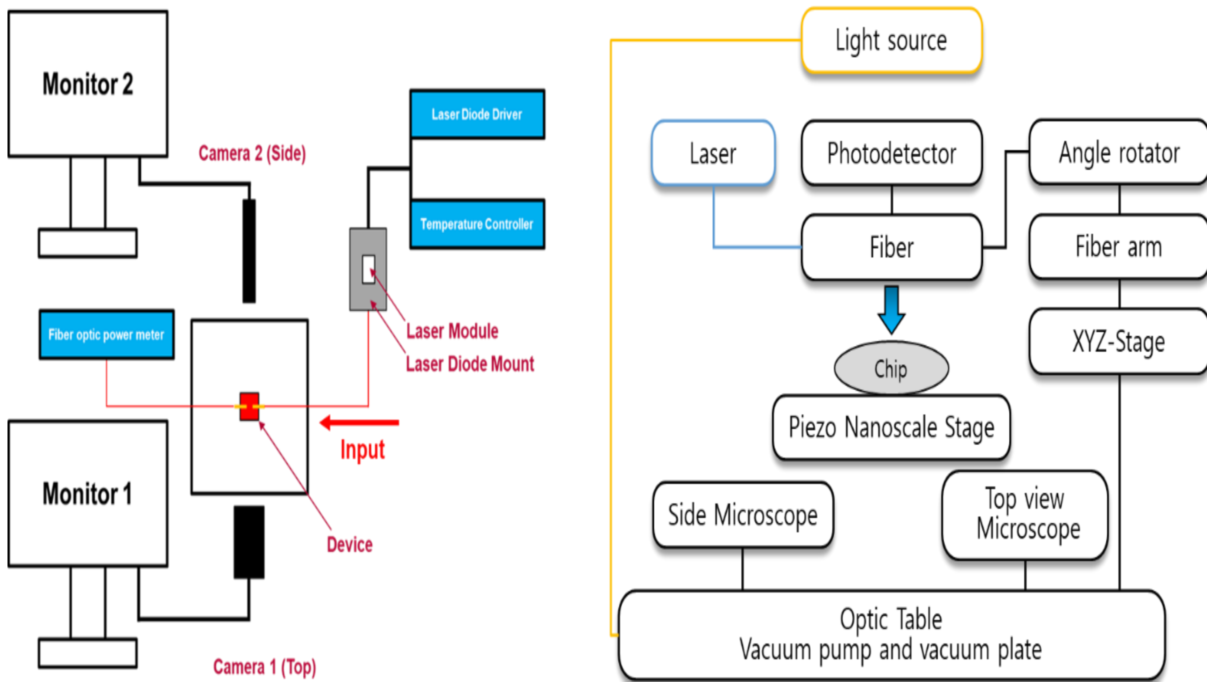


Figure 3.11: Schematic diagram of the experimental setup.

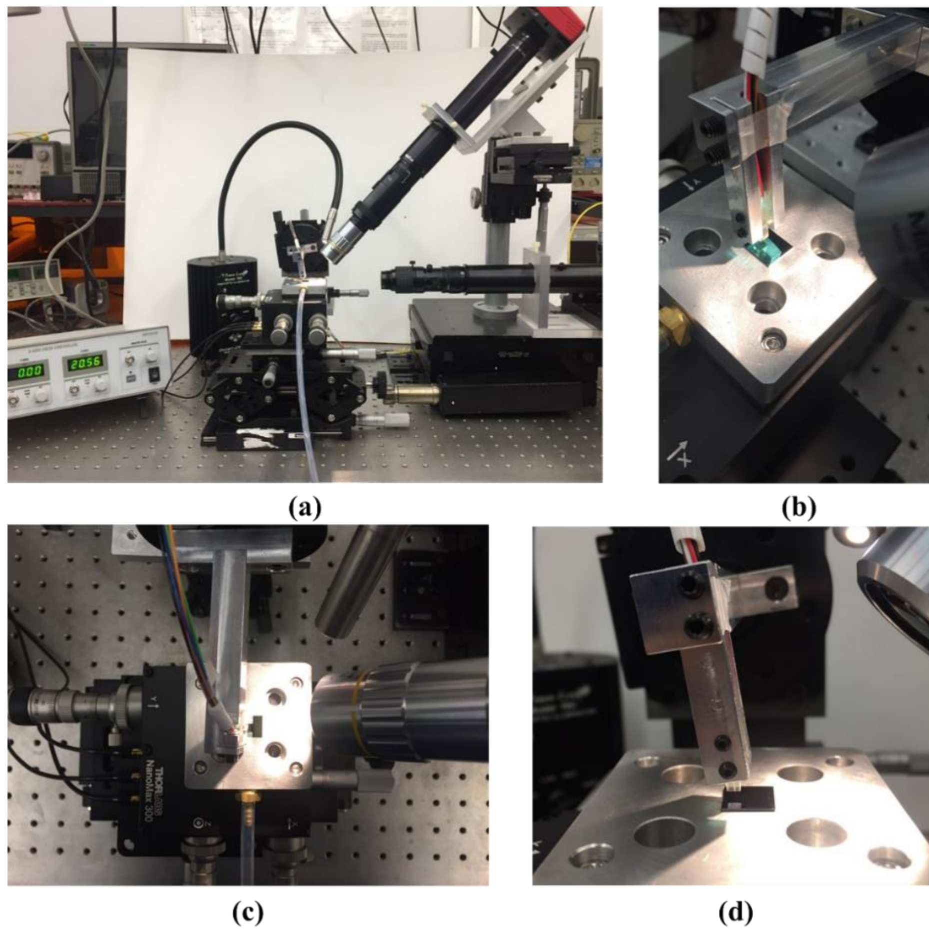


Figure 3.12: (a) Experimental setup of hybrid optical integrator and (b), (c), (d) close view of fiber array and SiPh.

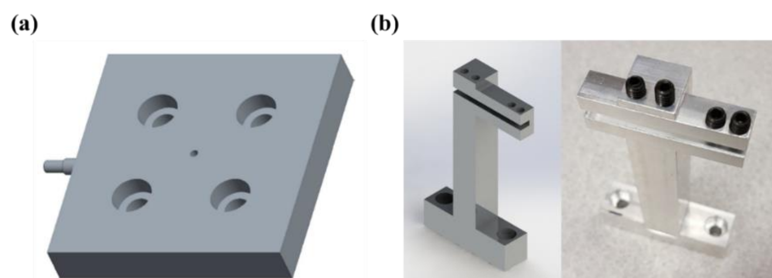


Figure 3.13: Custom designed part for the SiPh experimental setup; (a) vacuum plate and (b) fiber array holder.

Two cameras were used, and the specification of the cameras are shown in Figure 3.14 and Table 3.4. The top-view camera is tilted approximately 45 degrees to prevent other compartments block the observation of the grating coupler and the fiber. The top-view camera is designed to have higher magnification to observe the location of grating coupler accurately. The side-view camera is used to determine the distance between the grating coupler and the fiber, which does not require as high magnification as the top-view camera does.

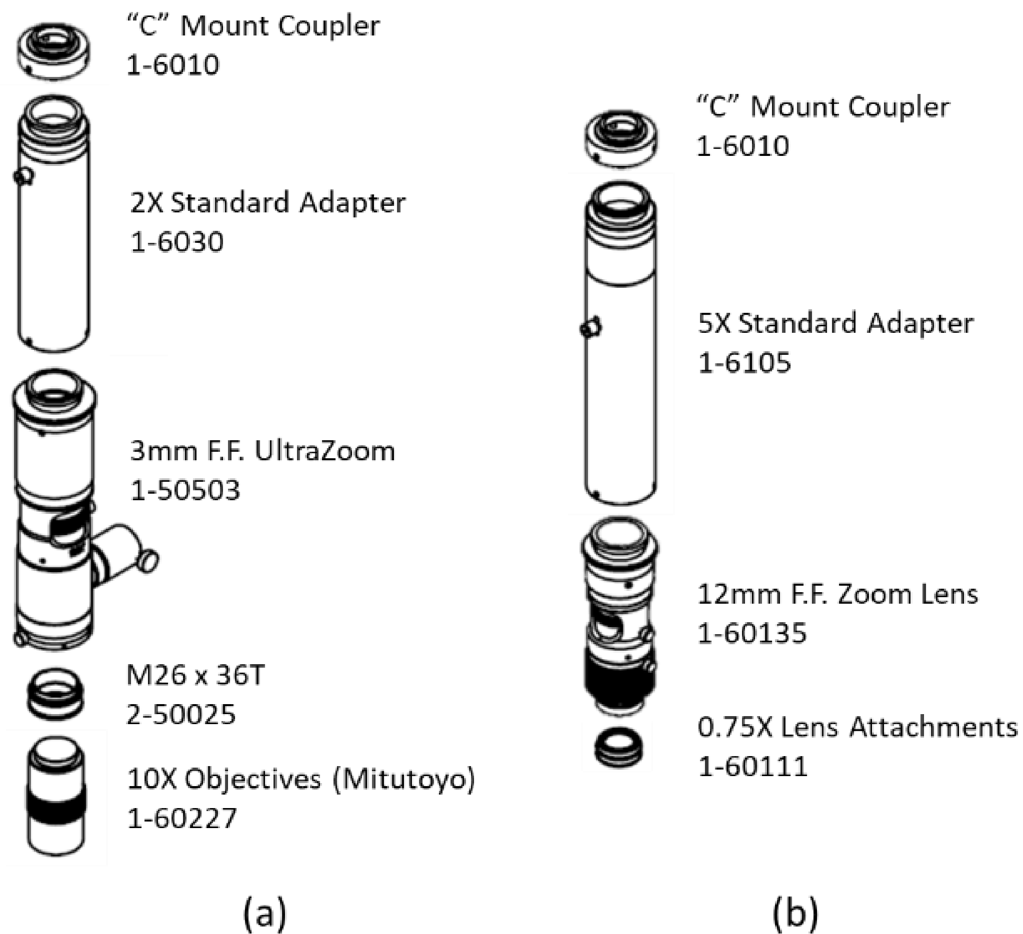


Figure 3.14: Schematic diagram of the CCD camera lens system; (a) for the top-view camera and (b) for the side-view camera.

Table 3.4: Specification of two cameras for the alignment process.

	Top-view camera		Side-view camera	
	Min.	**Max.**	**Min.**	**Max.**
Magnification	5.54 X	66.63 X	2.63 X	16.88 X
Numerical Aperture	0.28		0.053	
Resolve Limit (μm)	1.19	–	6.28	–
Working Distance (mm)	33	–	113	–
Field of View (mm)	3.05	4.07	0.12	1.44

Before proceeding further with the experiment, the insertion loss of fiber array was determined. The fiber array and fiber cable were precisely aligned with the assist of two CCD cameras as shown in Figure 3.15. The input power of 1.0 dBm from the laser driving current of 80 mA was used to measure the insertion loss of fiber array. It was determined that the fiber cable itself has loss of 1.73 dB. The measurement was completed five times for each port to characterize the loss occurred at the fiber array accurately. Figure 3.16 and Table 3.5 show the insertion loss of the fiber array for each channel.

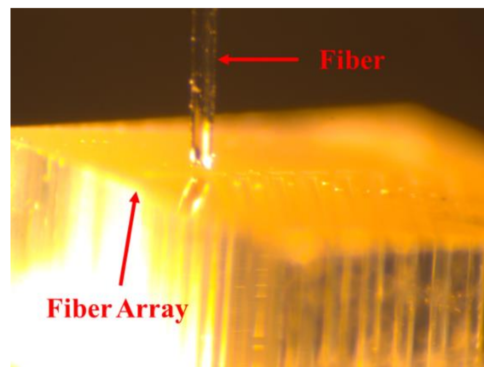


Figure 3.15: CCD camera image of fiber and fiber array for the insertion loss measurement.

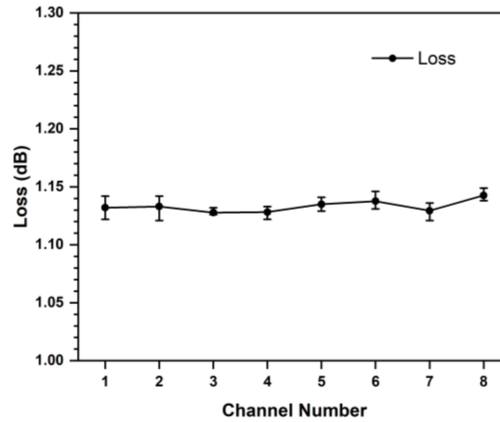


Figure 3.16: The insertion loss of fiber array port.

Table 3.5: The insertion loss of the fiber array channel.

Channel	Insertion loss (dB)
1	1.132 ± 0.1
2	1.133 ± 0.12
3	1.128 ± 0.14
4	1.128 ± 0.16
5	1.135 ± 0.16
6	1.138 ± 0.14
7	1.130 ± 0.14
8	1.143 ± 0.12

After the specification of the insertion loss of the fiber array was determined, the insertion loss of grating coupler was also determined with a broadband light source (Agilent 83437A). A schematic diagram of the experiment is shown in Figure 3.17 and the profile of input source is shown in Figure 3.18(a). Figure 3.18(b) shows the output from the two grating couplers and one Y-branches where – 3 dB loss occurs. Assuming that two grating couplers have the same insertion loss as the Y-branch leads to – 3 dB loss, the insertion loss of one grating coupler can be calculated

and the result is shown in Figure 3.19(b). The simulation result shows that at the wavelength of 1550 nm, the insertion loss is approximately – 3 dB, however, the experimental result shows approximately -10 dB insertion loss.

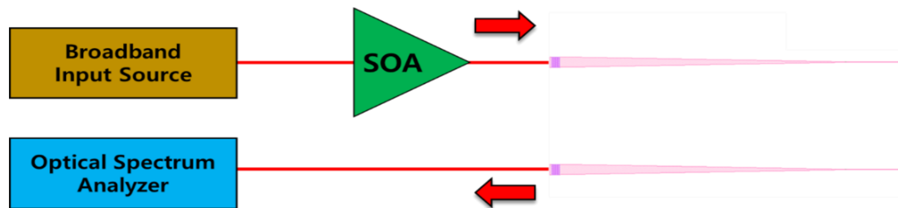


Figure 3.17: Schematic diagram of an experiment for grating coupler specification.

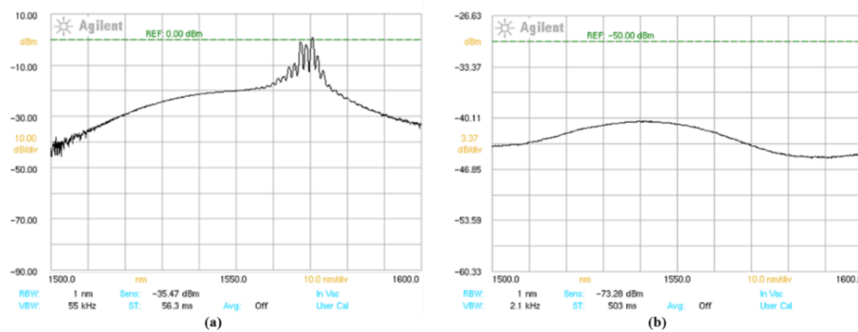


Figure 3.18: OSA image of (a) broadband input source and (b) output of two grating couplers.

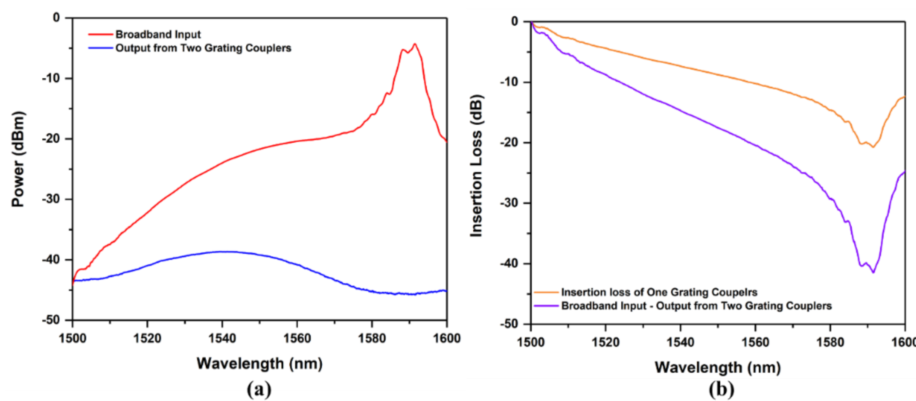


Figure 3.19: (a) Broadband input source and the output from two grating couplers, and (b) insertion loss of the grating coupler.

An additional experiment was performed to determine the optimum incident angle of the grating couplers. With the same setup shown in Figure 3.17, the angle of fiber normal to the grating coupler was changed from 7° to 13° by 1° increment. Figure 3.20 shows the broadband input source and the experiment result. Different from the simulation, the optimum angle of incidence is 11° ± 0.5°. In the case of 11° incident angle, the output power from two grating couplers and one Y-branch was highest, approximately -79.99 dBm. The exact insertion loss of each incident angle as a function of wavelength was also calculated by subtracting the output power (Figure 3. 20(b)) from the broadband input source (Figure 3.20(a)). Figure 3.21 shows the insertion loss of one grating coupler according to the incident angle. From the experiment, the optimum incident angle was determined to be 11° ± 0.5° with an optimum wavelength of approximately 1533. 4 nm ± 1 nm. The detailed reasoning for the difference between the simulation and the experimental result will be discussed in Section 5.

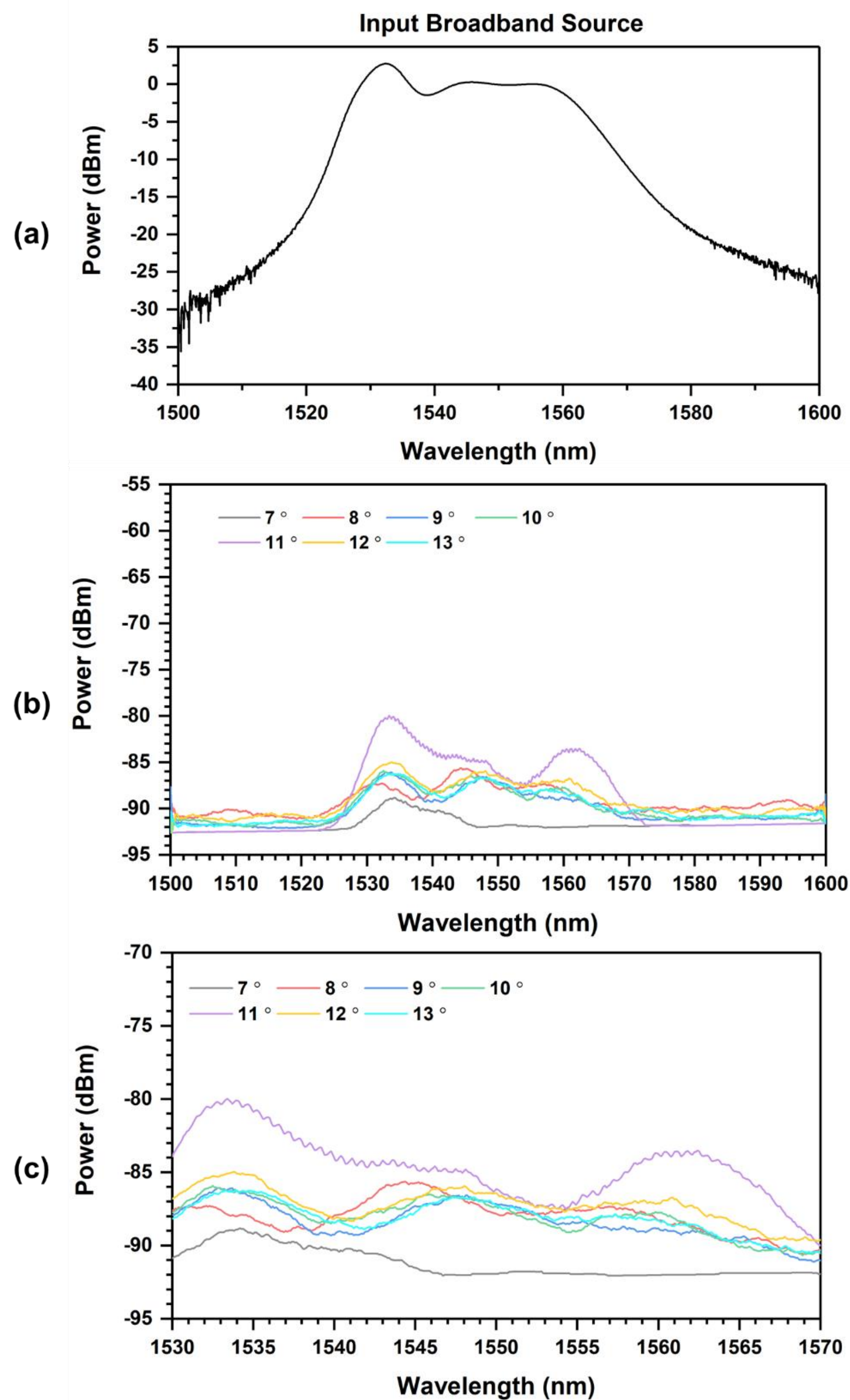


Figure 3.20: (a) Broadband input source and (b) output power of two grating couplers and one Y-branch and (c) magnified view of (b).

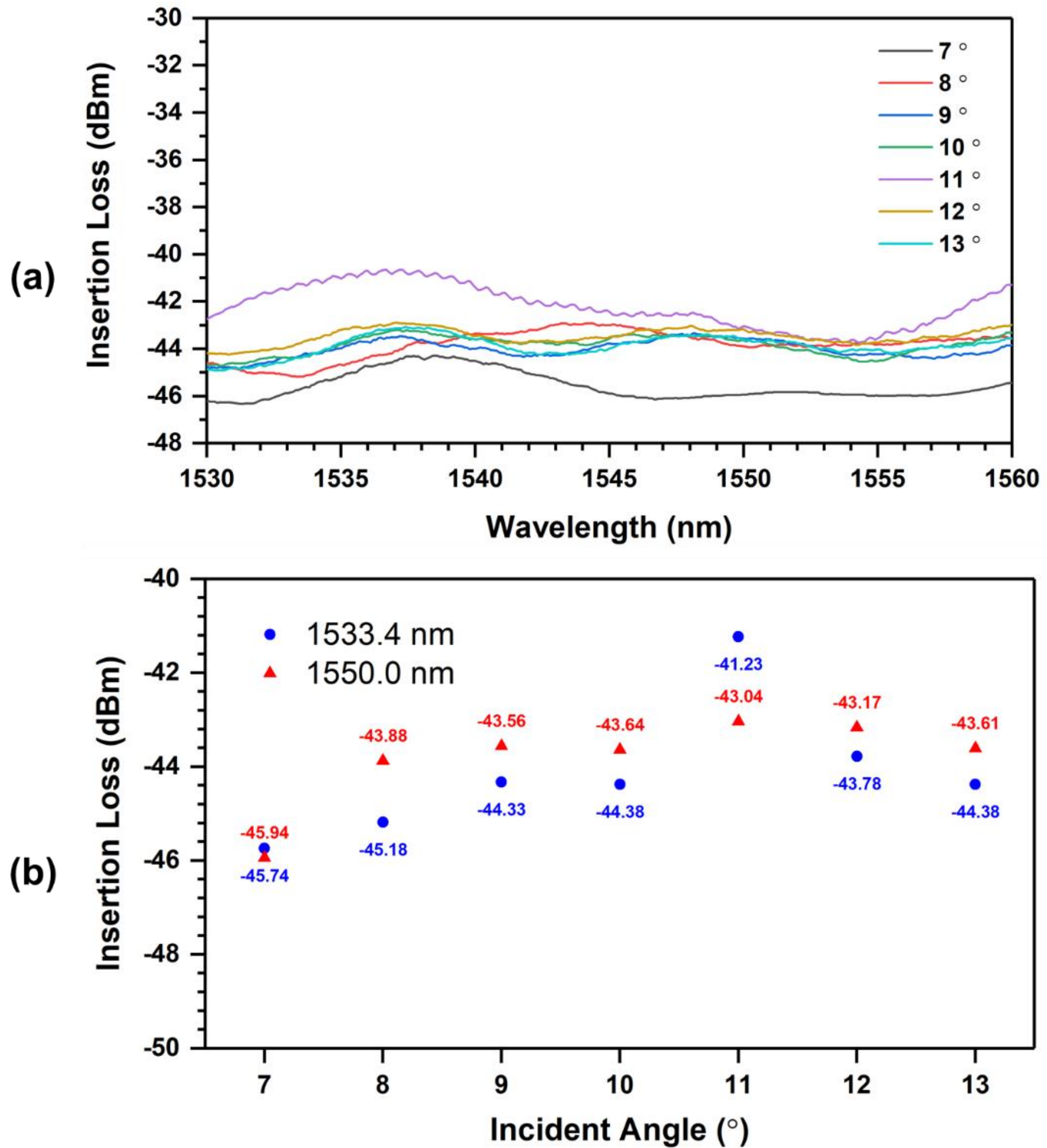
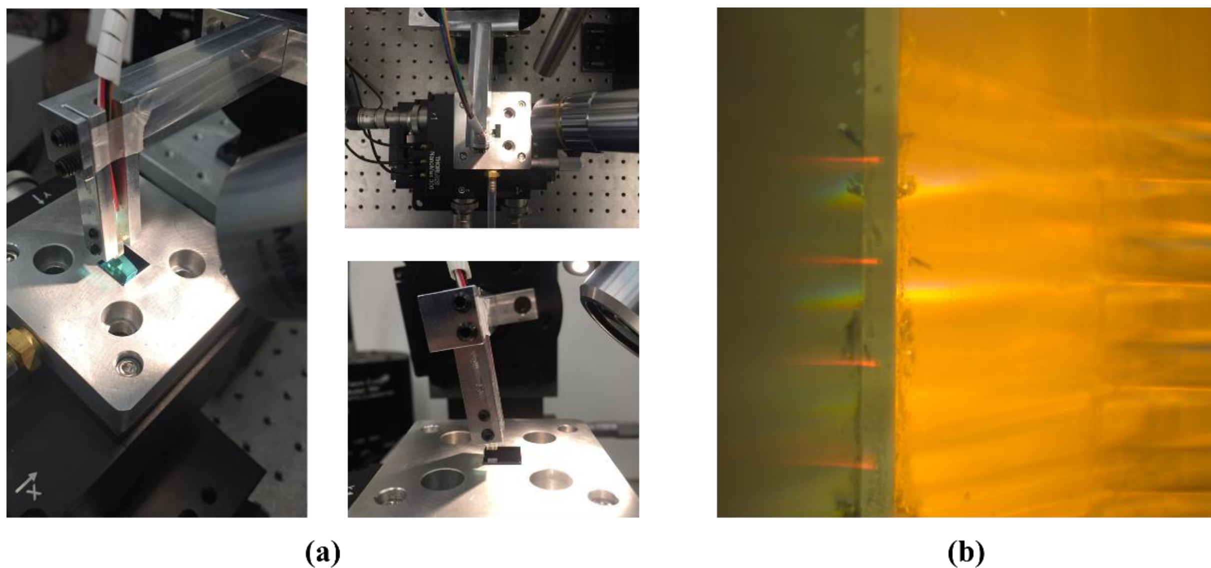


Figure 3.21: The insertion loss of one grating coupler via (a) wavelength from 1530 nm to 1560 nm and (b) two specific wavelengths: design wavelength (1550 nm) and optimum wavelength from experiment (1533.4 nm).

With two observation screens from two cameras and the nano-piezo stage, the grating coupler and fiber array were roughly aligned. Figure 3.22(b) shows the CCD camera image of the roughly aligned grating coupler and fiber array. After the rough alignment of two components, precise alignment was achieved by measuring the output power from the grating coupler using power meter (FPM-8210, ILX Lightwave) and OSA (Agilent 86140B, Agilent) to determine the optimal location of grating coupler selective to fiber array. When the alignment of the fiber array and the grating couplers was completed, the fiber array was connected to CW-EAM, SOA, a band-pass filter, an optical isolator, a photodetector, and an oscilloscope to determine the performance of the designed SiPh chip (Figure 3.23(b) and (c)).



(a) **(b)**

Figure 3.22: (a) Alignment of fiber array and SiPh die and (b) CCD camera image of the roughly aligned grating coupler (red structure) and fiber array (yellow structure).

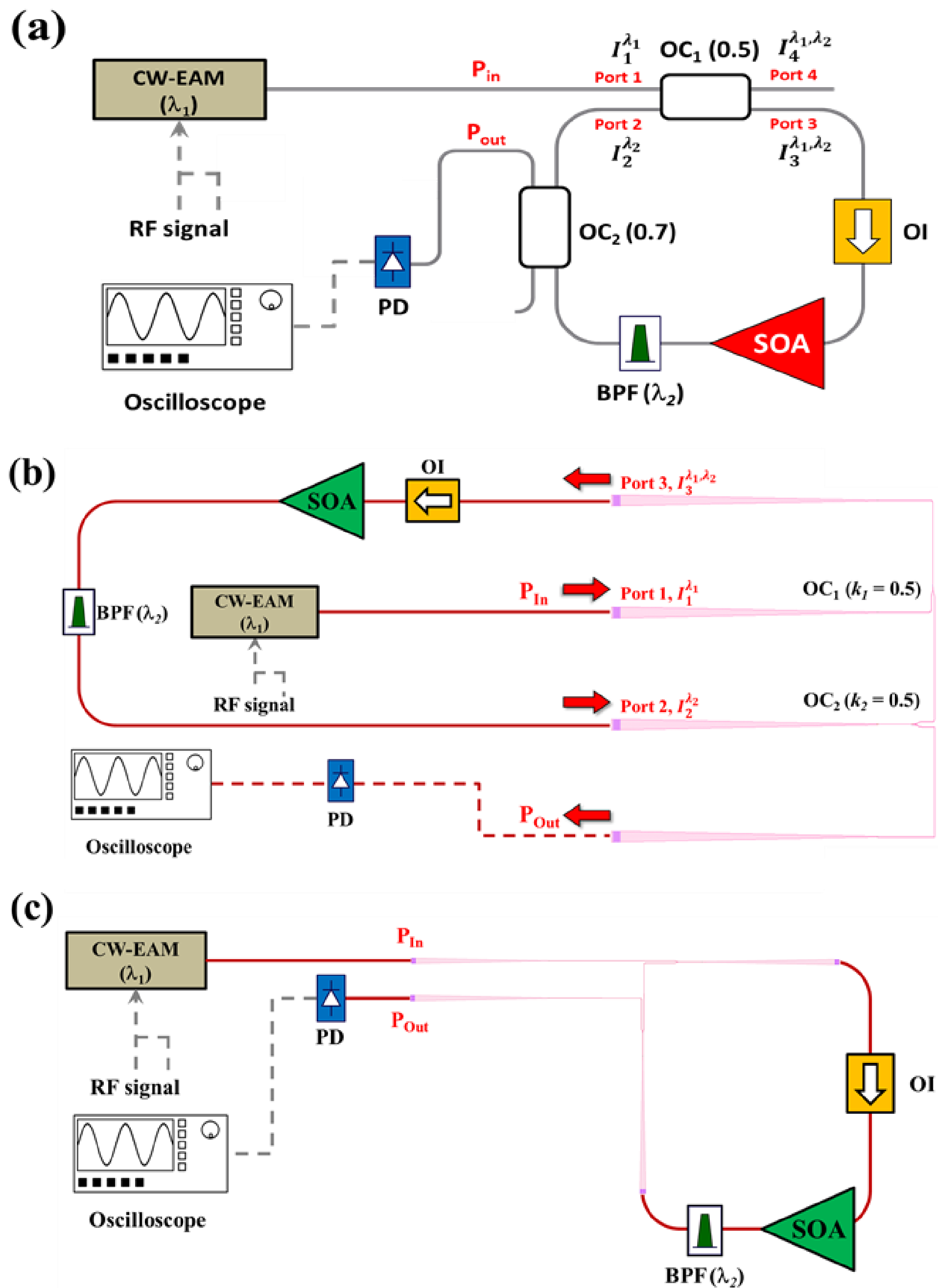


Figure 3.23: Schematic diagram of the optical integrator with three different sets of experimental arrangements based on (a) fiber optics setup and (b), (c) Silicon Photonics device with fiber optics components.

4. DATA ANALYSIS

4.1 Fiber-Optic Integrator

First, the proposed optical integrator system was evaluated and validated with a fiber optics setup. An optical integrator was constructed and characterized as shown in Figure 3.18. An input signal with a wavelength of 1553.95 nm (λ_1) to the OC_1 was generated using the laser source CW-EAM (FLD5F10NP, FUJITSU). The CW laser parameters was set as follows: 75 mA driving current and 27 °C TEC temperature with 1 dBm output power and 1553.3 nm peak wavelength. The optical carrier signal was intensity modulated with a square waveform at 1 MHz and a 1.5 V peak-to-peak value, with a + 1 V offset via a Agilent signal generator. A 50/50 optical coupler was placed right after the CW-EAM to propagate half of the input signal in the optical loop constructed by the SOA, BPF, OI and 70/30 optical coupler. The input signal with the intensity of $I_3^{\lambda_1}$ first went into the SOA that is lower than its saturation power in order to achieve a linear response. The signal was then bandpass-filtered to define the circulating wavelength of 1551.00 nm (λ_2). To prevent any back-reflection of signals and reduction of the noise signal in the optical loop, an optical isolator was introduced within the loop. The 70/30 optical coupler extracted 30% of the circulating signal as output signal. The length of the optical-fiber loop is approximately 10 m. According to Eq. (2.7) and (2.12), the free-spectral range (FSR) and the sampling period can be calculated as $FSR \approx 20$ MHz and $T \approx 50$ ns, respectively. The performance of the system was determined by the output signal extracted by 70/30 optical coupler connected to the photodetector (DET01CFC, Thorlabs) and oscilloscope (Agilent 54621, Agilent) as shown in Figure 3.23(a).

Figure 4.1(a) shows the output signal of fiber-optic integrator measured by an oscilloscope. Using a square-shaped input signal with a frequency of 1 MHz, a good agreement between the experimental measurements and the numerical simulation result was observed (Figure 4.1(b)). The calculated value of the sampling period was approximately 50 nanoseconds (ns). Figure 4.2 is in agreement with this value, showing a sampling frequency of 54 ns. An input frequency of 1 MHz allows for 10 discrete steps within each rise and fall of the signal with 50 ns sampling period (10^9 / (2 · 1 MHz · 50)), and experimental results show approximately 10 discrete steps. Figure 4.1(c) and (d) shows the experimental result with different input signal frequency of 500 kHz and 2 MHz, respectively. With an input frequency of 500 kHz, the output signal shows more discrete steps, 20 steps (10^9 / (2 · 500 kHz · 50)), compared with 1 MHz and 2 MHz. On the other hand, there is a fewer number of discrete steps, 5 steps at 2 MHz (10^9 / (2 · 2 MHz · 50)). Figure 4.2 shows the magnified view of Figure 4.1(a), emphasizing the nature of the integrated signal. The sampling period of the system, identical to the one-step period, is approximately 50 ns (T) with an FSR of 20 MHz which is in agreement with the simulation result. In addition, the change in the amplitude decreases from the lowest amplitude to the highest point. At the beginning of the sampling process, the gain of the non-linear SOA is selectively larger than the signal gain each round trip. As the signal starts accumulating, the amplitude of the input signal becomes larger, and the gain of the SOA decreases and eventually leading to a smaller step size. The effect of optical loop length is also demonstrated by decreasing the length from approximately 10 m to 7.5 m. The sampling period is decreased to 36 ns as shown in Figure 4.3 which is close to the theoretical value of 37.5 ns. From this experiment with fiber optics components, the proposed SiPh system can be constructed to perform as an optical integrator.

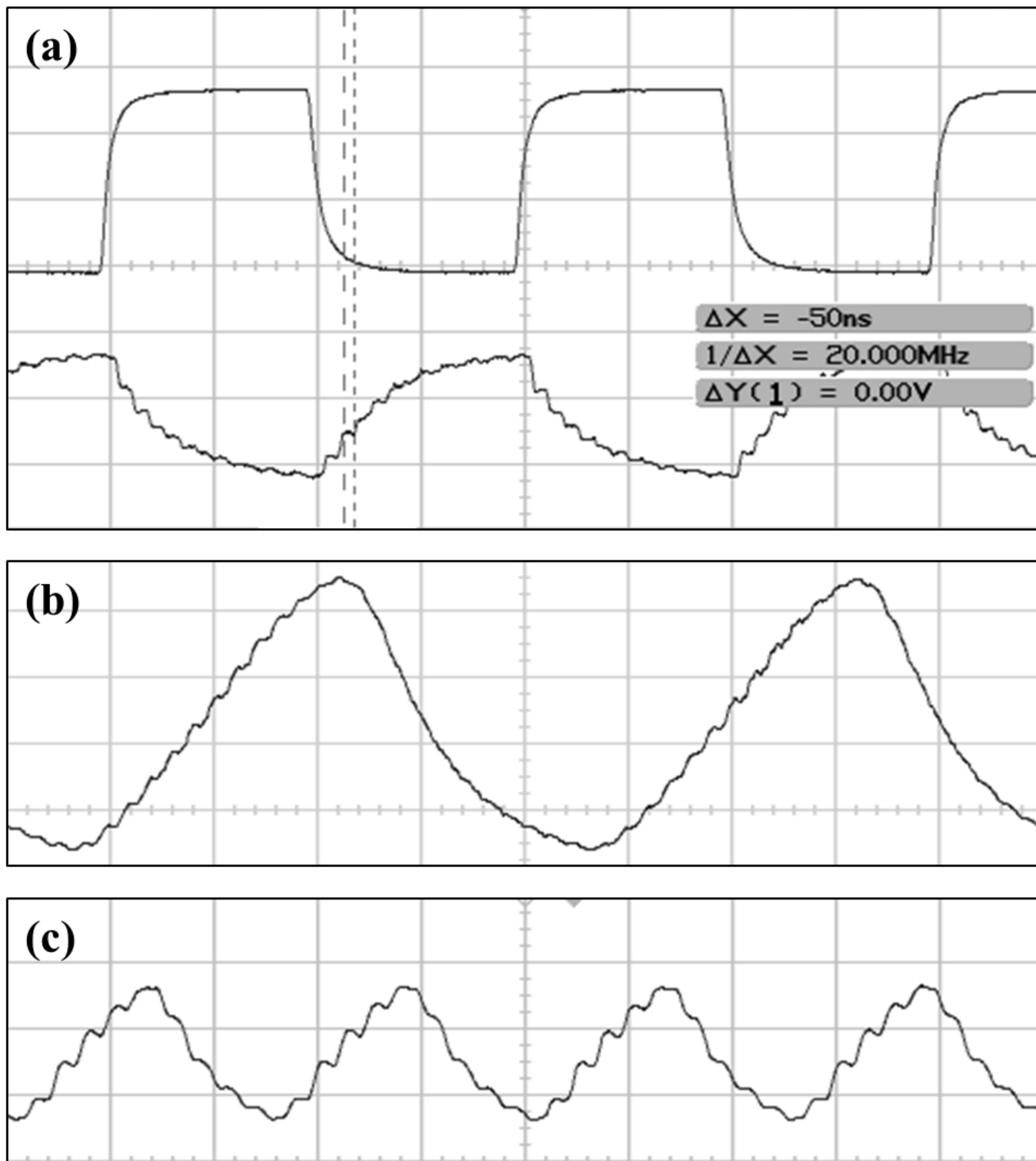


Figure 4.1: Experimental measurement of the optical integrator output signal with input signal frequency of (a) 1 MHz, (b) 500 kHz, and (c) 2 MHz.

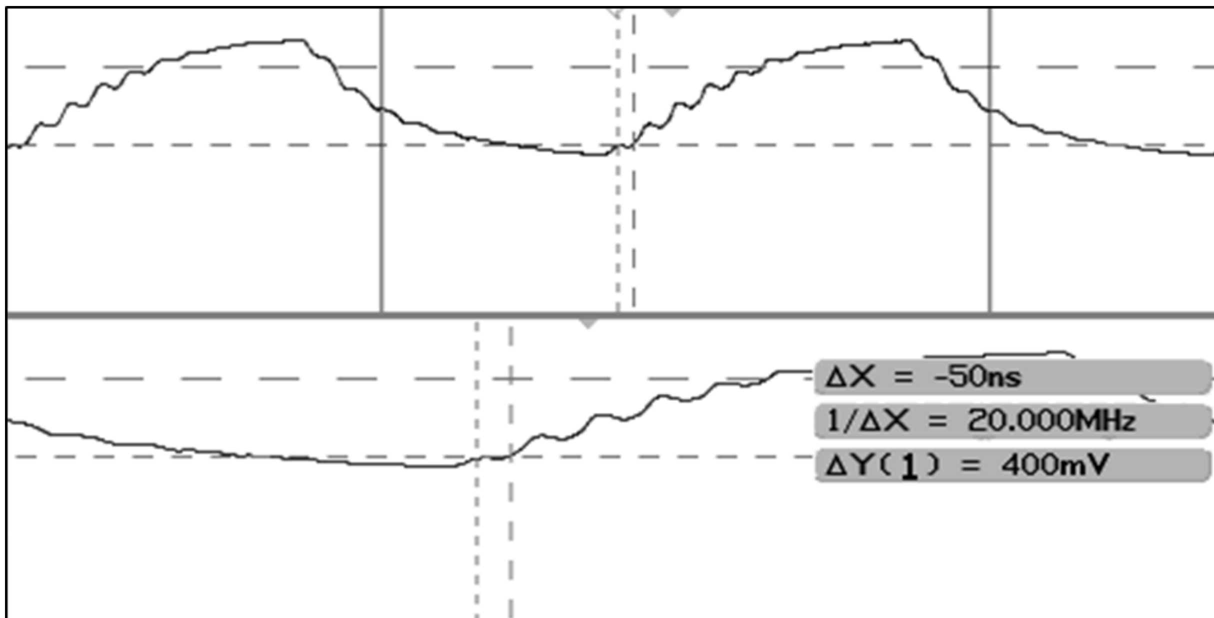


Figure 4.2: Zooming oscilloscope view of discrete steps of the output signal at 1 MHz input signal.

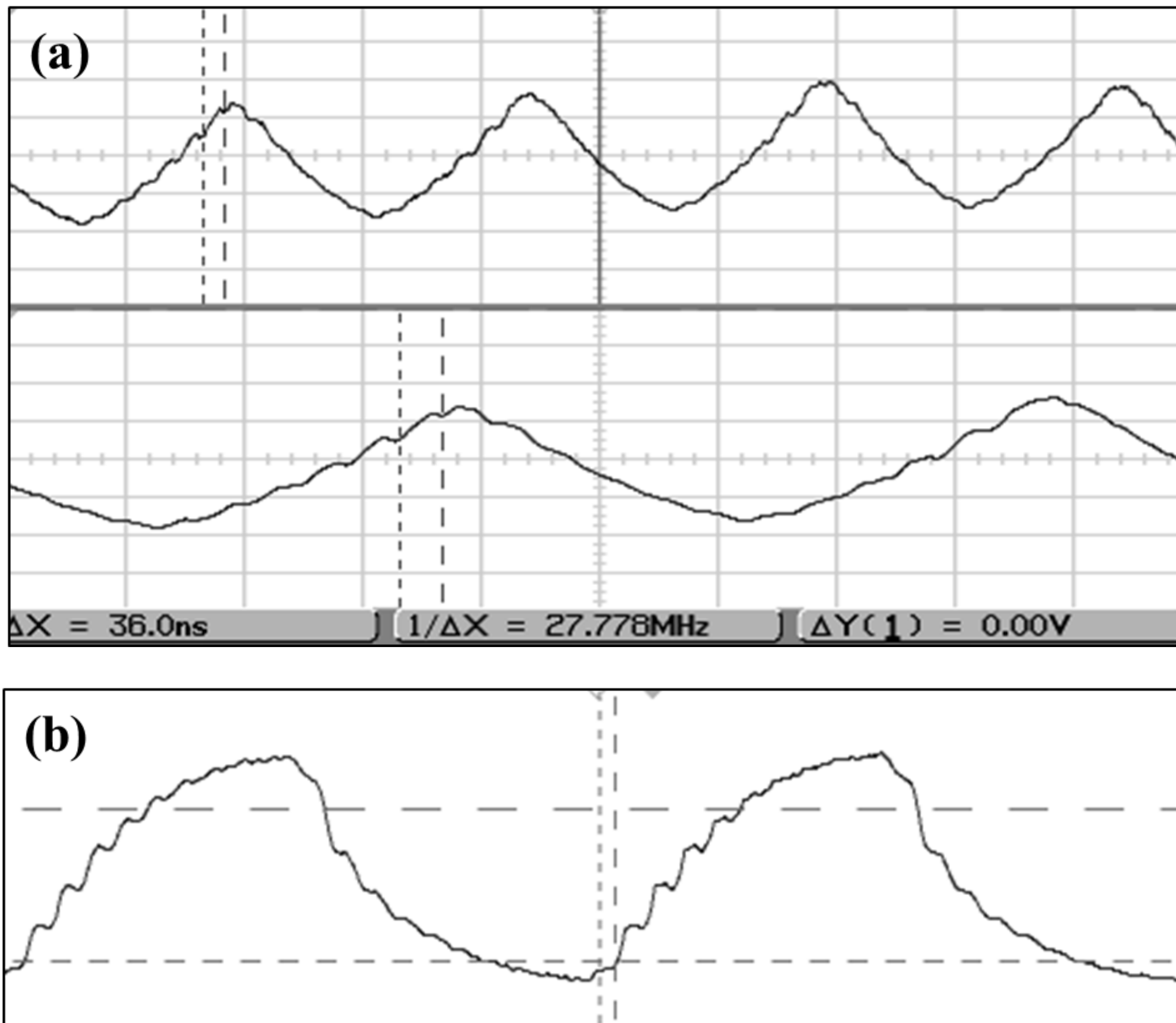


Figure 4.3: Experimental measurement of the optical integrator with an optical loop length of 7.5 m and input signal frequency of (a) 2 MHz and (b) 1.5 MHz.

4.2 Hybrid Optical Integrator

The alignment of the fiber array and grating couplers are performed as described in Section 3.2.2. After the alignment, the experiment is performed as described in Figure 4.4. The optical loop length of the system is approximately 5m, which includes the SiPh devices waveguide and optical-

fiber components. The free-spectral range and the sampling period can be calculated as $FSR \approx 40$ MHz and $T \approx 25$ ns based on Eq. (2.7) and (2.12). Due to the severe insertion loss from the silicon photonics grating couplers, the driving current of the CW-EAM and the SOA are set to their maximum value. The CW laser is set to 150 mA driving current and 27 °C TEC temperature with 3.1 dBm output power and 1553.3 nm peak wavelength. The driving current of the SOA and TEC temperature are set to 500 mA and 25°C, respectively. Figure 4.4 shows the schematic of the hybrid optical integrator with the fiber array and its corresponding channel numbers. In Figure 4.4, the circled numbers indicates the fiber array channel number, and the circled letters indicate the grating couplers. The CW-EAM is connected to the fiber array channel 2, and the modulated input signal is coupled to the grating coupler B. Then the signal is propagated through grating coupler B, the Y-branch and the grating coupler A (located under the fiber array channel 1). The signal from grating coupler A is then coupled to the fiber array channel one, which is connected to the input port of the optical isolator. The optical signal propagates through the optical isolator SOA, the bandpass-filter, and fiber array channel 3. The signal from fiber array channel 3 is coupled to grating coupler C. Half of the signal is coupled to the grating coupler C and then to grating coupler A to complete its circulating optical loop. The other half of the signal is propagating to the grating coupler B and extracted to the fiber array channel 4 as an output signal. The output signal of hybrid optical integrator is detected and observed using a photodetector and an oscilloscope.

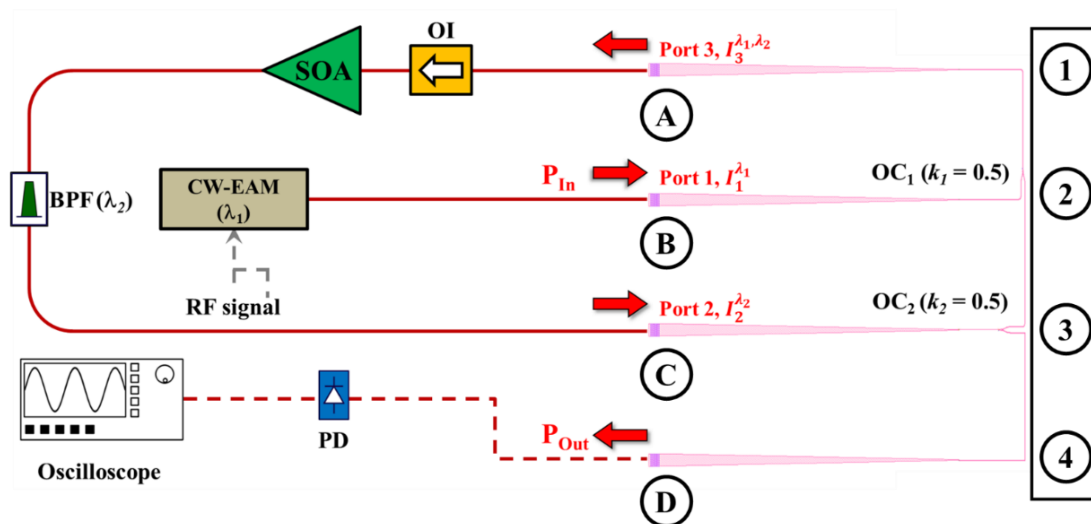


Figure 4.4: Schematics of the experimental setup for the hybrid optical integrator.

Figure 4.5 shows the output signal of the hybrid optical integrator as measured by an oscilloscope. With a square-wave input signal of frequency 1 MHz, the output signal shows 10 discrete steps for each rise and fall of the signal (10^9 s / (0.5 · 1.8 MHz · 28)), which can be observed with the sampling period T of an approximately 28 ns (Figure 4.5(a) and Figure 4.6(a)). At a frequency of 0.9 MHz, approximately 20 discrete steps for each rise and fall of the signal can be observed as shown in Figure 4.5(b). The peak-to-peak voltage of the output signal from the hybrid optical integrator is approximately 1.75 mA, which is significantly smaller than that of the fiber-optic integrator of approximately 421 mA (Figure 4.2). Due to the large insertion losses of silicon photonics devices, and additional propagation loss, the driving current of the laser and SOA must be maximized in order to obtain an appropriately shaped output signal. In addition, the modulated signal amplitude must be increased from 1.5 V to 2.5 V.

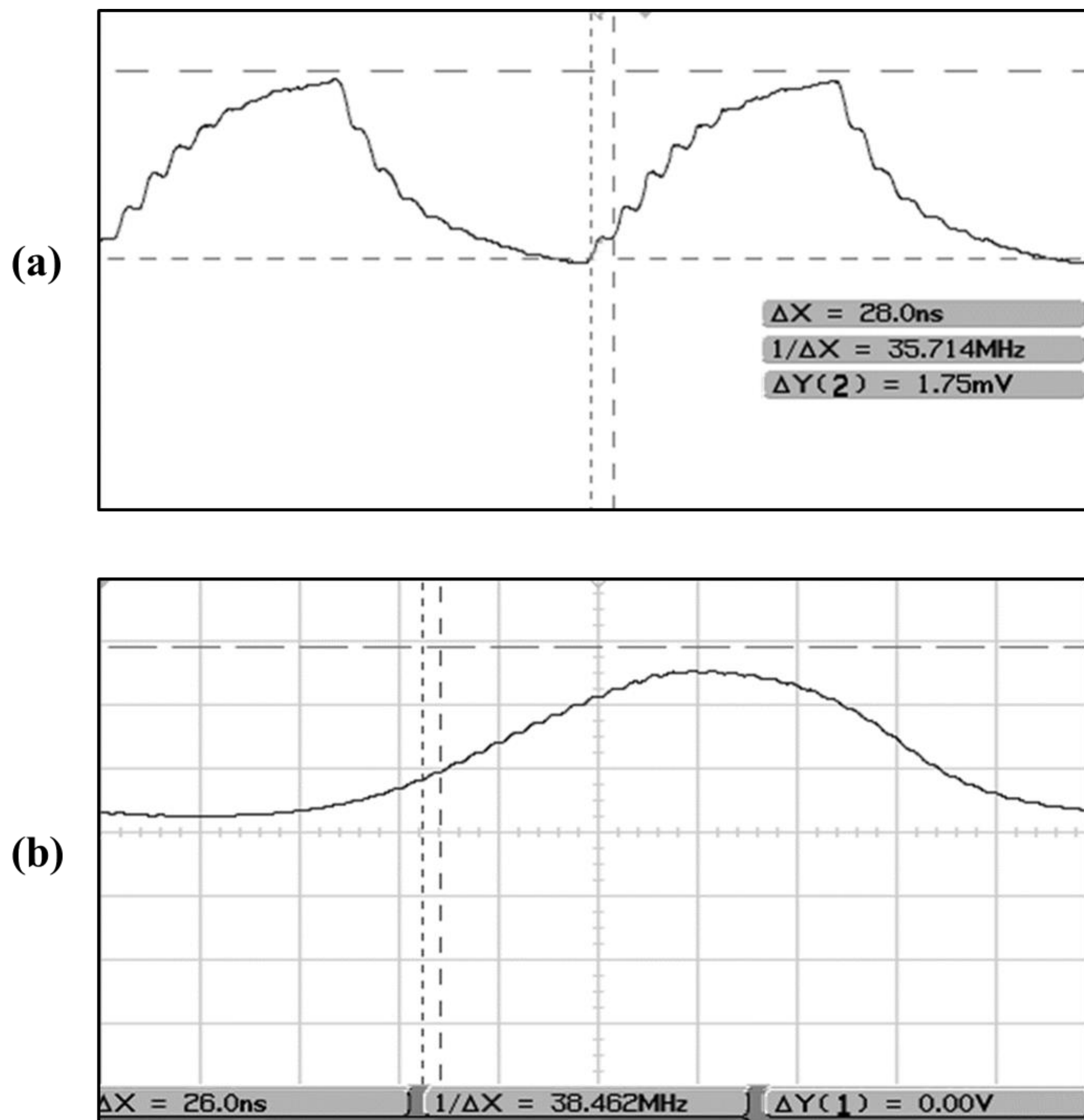


Figure 4.5: Experimental measurement of the optical integrator output signal with an input signal frequency of (a) 1.8 MHz and (b) 0.9 MHz.

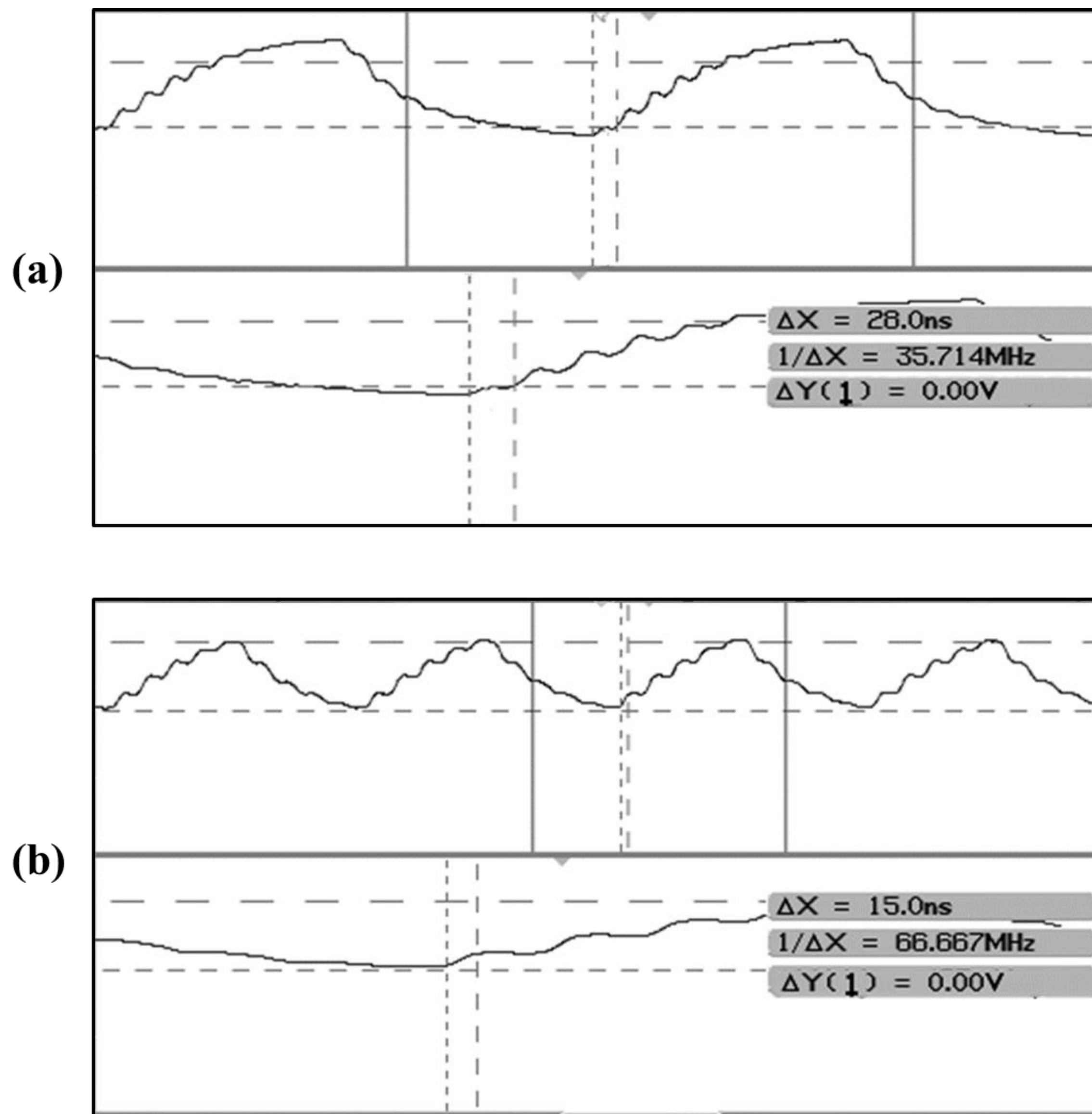


Figure 4.6: Zooming oscilloscope view of the discrete steps of the output signal at an input signal frequency of (a) 1.8 MHz and (b) 3.6 MHz.

5. DISCUSSIONS

5.1 Alignment of Fiber Array and Grating Coupler

The most challenging part of this project is coupling light into the silicon grating couplers. The accurate positioning of two components is one of the difficulties faced during the experimentation. The cross-sectional area of an optical fiber core (diameter of 6-9 μm) and the cladding (diameter of 125 μm) is approximately 600 times larger than that of the grating couplers (12 × 14 μm^2). In addition, the fiber core is located at the center of the fiber array, which gives additional difficulty to align the fiber-array on the center of the grating coupler due to the limited observation space of the two cameras. Proper control of the external light source for the CCD camera and adjustment of the camera focus also limits viewing of each part of the fiber array and the grating couplers. A slight misalignment, tilt or rotation of a stage can affect the alignment procedure and directly lead to substantial insertion loss. Due to the difficulty of controlling the incident angle additional simulation is done to determine the effect of the angle and transmittance of the grating coupler as shown in Figure 5.1. The simulation result indicates an angular difference of ± 0.5° does not decrease the coupling efficiency substantially. As such, the rotational stage was fixed for the optimal incident angle of the fiber array, 8° ± 0.5°. Although most of the anticipated errors are considered, there are still errors due to the assembly of the parts which cannot be detected by the naked eye or the CCD camera due to limited resolution and the working distance of the lens system. As such, we divided the alignment process into two steps: the rough alignment of the fiber array and the grating couplers supported by the camera. and then the precise alignment using a nano-piezo stage and power measurement from the grating couplers. One of the fiber array channels is

connected to the CW-EAM laser, and then this channel is placed on one of the grating couplers in the SiPh die. The optical source propagates through the waveguide and one grating coupler in order to couple to one of the fiber array channels which is connected to the OSA. The optimum position of the SiPh die is determined by the OSA monitor that shows the maximum optical power. This process approximately takes one hour to align the fiber array and the grating coupler. However, it is possible that better alignment can be achieved using a more sophisticated stage or spending more time for the precise alignment. Nowadays, most of this alignment procedure is done automatically, and it will be described in Section. 6.2.

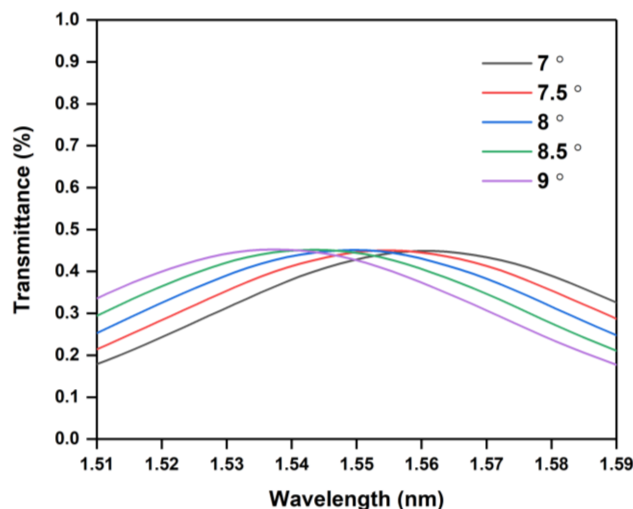


Figure 5.1: The transmittance of the grating coupler for different angles of incidence.

5.2 Fabrication of Silicon Photonics Device

From the experimental result of the grating coupler insertion loss, there is an additional loss which we expected from the simulation result. Our design aimed for – 3 dB insertion loss, while experiment shows approximately – 10 dB loss. Due to a massive difference between these two

results, more detailed inspection of fabricated was carried out. There were several issues detected after inspection of Silicon Photonics device fabricated using E-beam lithography which can be the cause of additional loss and shift of the optimal wavelength. The SiPh devices were inspected using scanning electron microscopy (SEM) and atomic force microscopy (AFM). To perform measurements using the AFM (MFP-3D, Oxford Instruments), AC mode was used with a resonance frequency of AFM tip as 72.078 kHz is selected as the measurement method. An AFM tip with a tip radius of 7 nm is used and the detail image and specification is shown in Figure 5.2 and Table 5.1. Using the AFM, the dimension of the structure, the roughness of the surface, and the edge of the structure can be measured in order to evaluate the quality of fabrication. From the inspection, three issues were detected which are listed below:

1. Wafer thickness and yield
2. E-beam over-exposure and alignment of the second exposure
3. Quality of nanostructure after the second etch

First, the variation of wafer thickness lowers the yield rate and reduces the number of useful devices that are fabricated. The initial SOI has a thickness variation of approximately 200 nm (Figure 3.7), and after the thinning process of the Si layer, only a limited area has a uniform thickness of 220 nm. As mentioned in Section 3.1.2, the thickness of Si layer before the E-beam lithography has a significant effect on the yield rate of the fabrication process. In addition, the device layer is designed to have a Si thickness of 220 nm for the fabrication process, otherwise the performance of the device will show a different result. To determine the effect of the Si thickness on the coupling efficiency of the grating coupler, additional simulation is done and the result is shown in Figure 5.3. Furthermore, the exposure and etch time during the E-beam lithography is

calculated based on the assumption that the thickness of the Si layer is 220 nm. As such, the device fabricated on the area with a different value of silicon thickness than 220 nm cannot be used for this project. For example, disconnection of the waveguide, or unexpected silicon residue can be observed when the thickness of Si is more than 220 nm as shown in Figure 5.4.

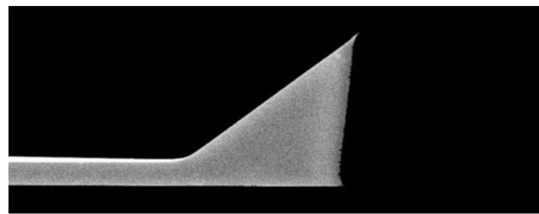


Figure 5.2: SEM image of AFM tip.

Table 5.1: AFM tip specifications.

Geometry	**Visible Apex**
Tip Height (h)	9.0 – 12 μm
Tip Radius (Nom)	7 nm
Scan Mode	AC mode

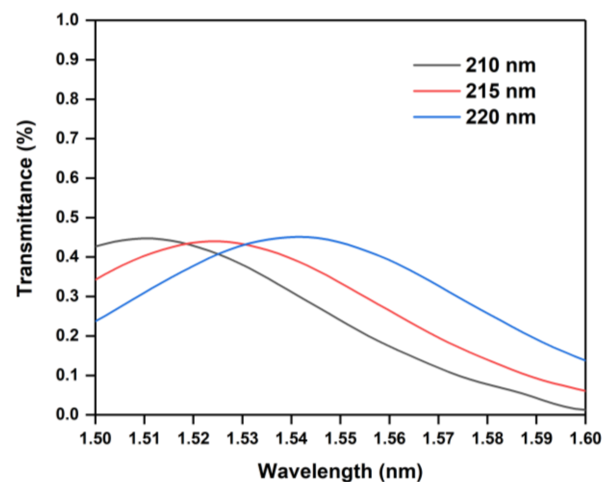


Figure 5.3: Transmittance of the grating coupler for different silicon layer thickness.

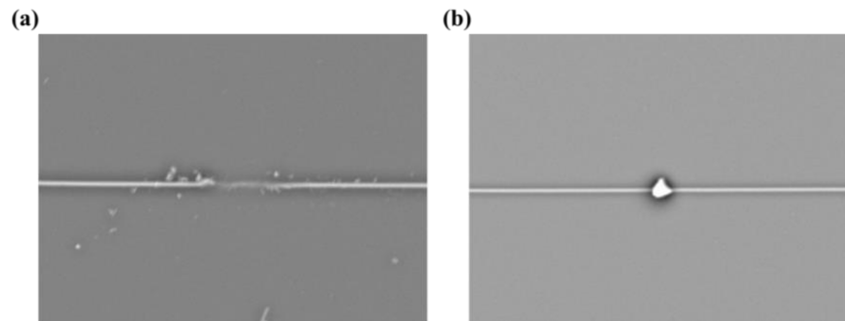


Figure 5.4: SEM image of (a) disconnected waveguide and (b) Si residue on the waveguide.

Second, the problem during the E-beam lithography process can be observed through SEM imaging of the SiPh devices. While inspecting grating couplers, misalignment of the second exposure is detected as shown in Figure 5.5. The SEM image shows that the edge of the grating coupler has space that is not etched away and trace of the exposure on SiO_2 can be found on the opposite side of the edge (Red box in Figure 5.5(a)). The over-exposure of E-beam can be observed as shown in Figure 5.5(b), where the dark area indicates the excessive exposure of the SiO_2. This area means that exposure time is longer than expected so that during the exposure process, the SiO_2 under the Si layer is also exposed by the E-beam.

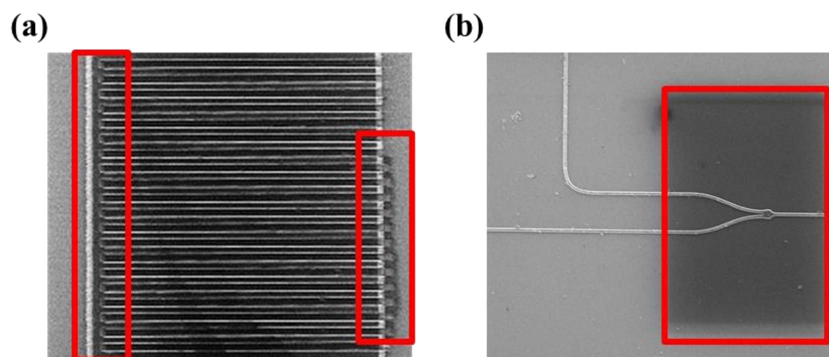


Figure 5.5: SEM image of (a) misalignment of the second exposure and (b) over-exposure of E-beam during the lithography process.

The quality of the E-beam lithography, such as surface roughness, resolution, and etch depth affect the performance of the fabricated device. The residue of photoresist can be detected between the gratings as shown in Figure 5.6(a). These defects can diffract the light and reduce the efficiency of light coupling into the grating coupler. Several cleaning processes using acetone and methanol are performed to clean the contaminants. However, it is difficult to remove all of the contanimants between the grating corrugations. The sidewall quality of periodic structure can cause a problem as well. The schematic diagram of the cross-section of gratings is shown in Figure 5.6(c). The desired structure has straight and perpendicular structure, while the fabricated device has round edges. The thickness of one round edge is approximately 50 nm which is 1/6 of the grating width (Figure 5.7). The grating width is approximately 304.8 nm which is very close to the design, 305 nm. However, this rounded edge possibly affects the coupling efficiency of the grating coupler. For example, the Bragg's condition discussed in Section 2.4.2 cannot be satisfied when the round edge could increase the diffraction angle, thus leading to a different incident angle from that of the design and simulation values. As shown in Figure 3.20, the optimum incident angle and wavelength is 11° and 1533.4 nm, respectively. The low quality of the fabrication leads to a different optimum value due to the experiment conditions. The surface roughness must be considered as one of the problems. The sidewall and surface roughness has a vast impact on light propagation [16]. As shown in Figure 5.8, it can be observed that a surface roughness for the waveguide and Y-branch is present. The surface defects can cause unexpected additional propagation loss during the experiment.

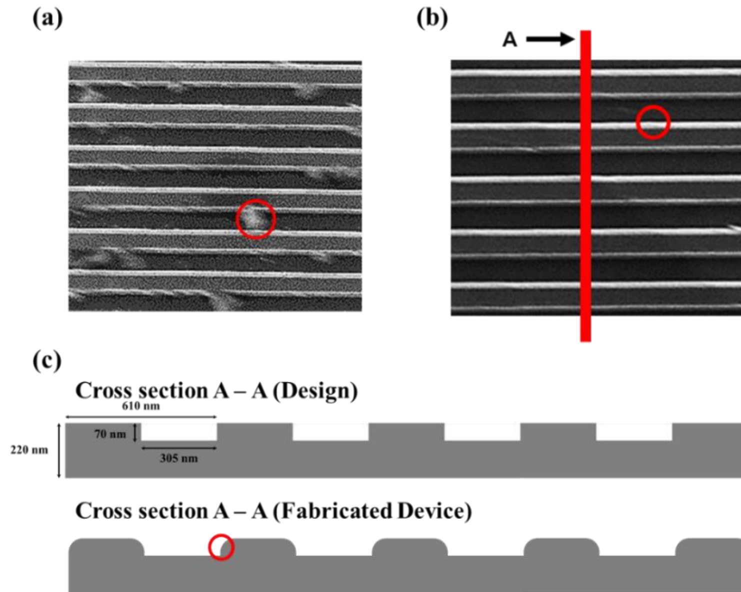


Figure 5.6: SEM image shows (a) contaminants after the etching process, and (b) gratings with the round edge, and (c) schematic diagram of the cross-section of the grating coupler.

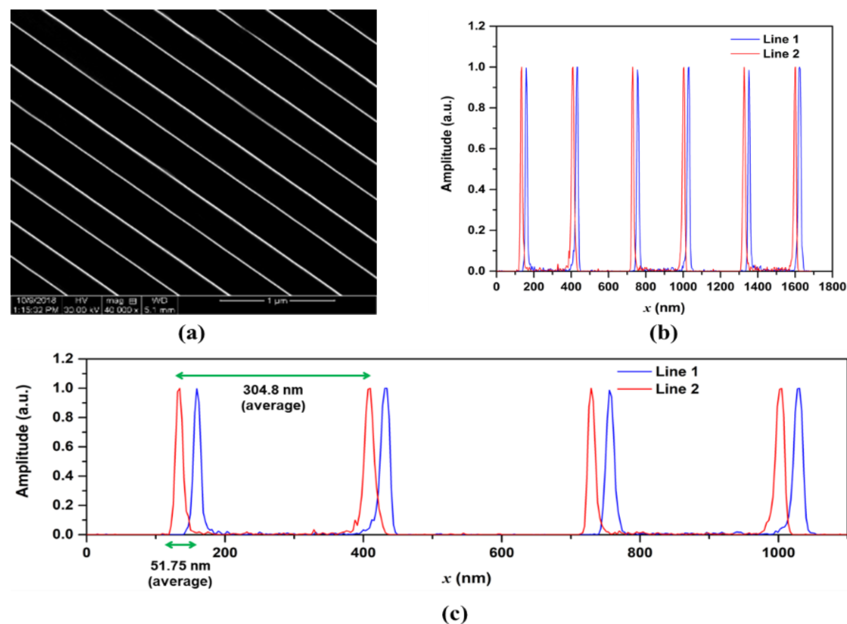


Figure 5.7: (a) SEM image of the grating coupler (40,000 ×), (b) measurement of the gratings period, the grating width and the round edge thickness, and (c) zooming view of (b).

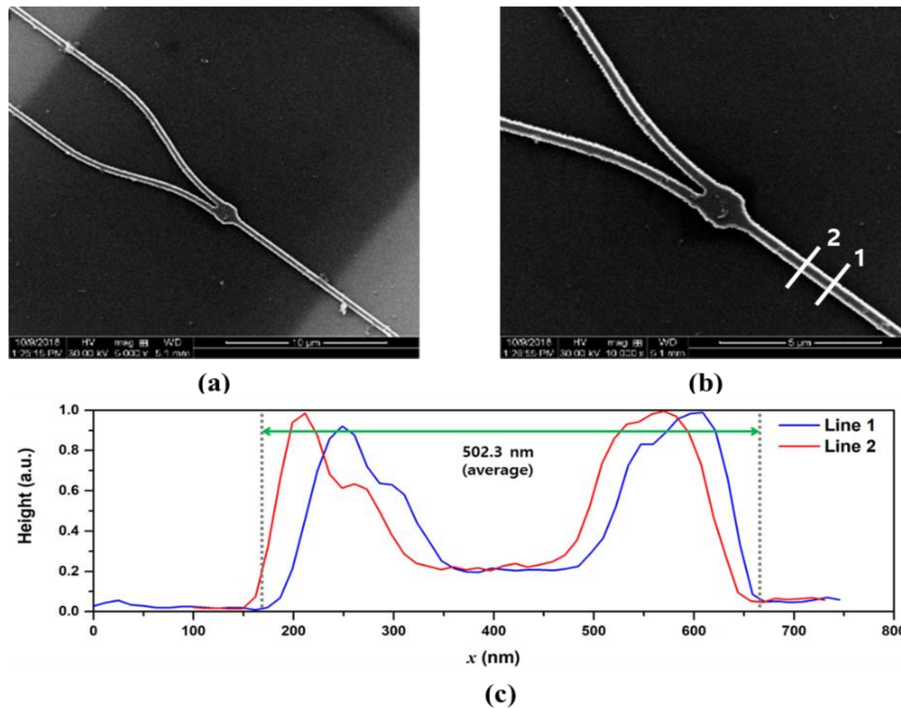


Figure 5.8: (a) SEM images of Y-branch and (b) its magnified image of (a), and (c) rough sidewall of the structure.

In addition, the design was changed due to the low resolution and imperfect process of the E-beam lithography. The initial design of the grating coupler was a focusing grating coupler with circular grating structure as shown in Figure 5.9. The advantages of this design include compact structure and reduced fabrication process and cost due to the small size of the grating coupler, 659.75 μm^2 (20.3 μm × 32. 5 μm) compared to a straight grating coupler, 4968 μm^2 (12 μm × 414 μm). However, the periodic structure of the grating coupler was not fabricated properly after the etching of the photoresist as shown in Figure 5.10(b). The round edge of the nanoscale periodic structure also showed the low quality of the sidewall. As a result, the design was changed to a straight grating coupler with a vertical length of approximately 413 μm.

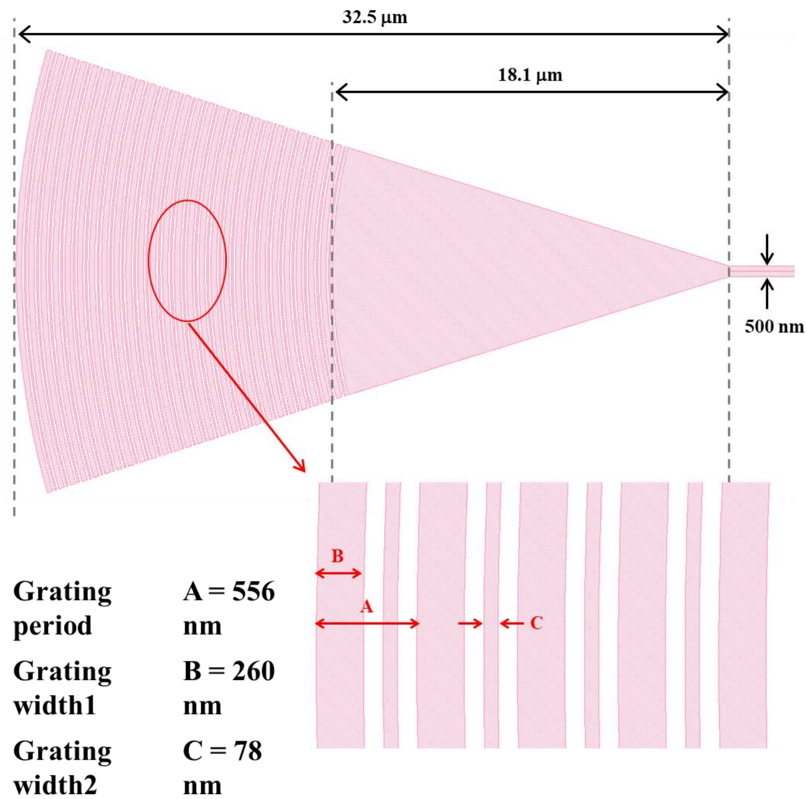


Figure 5.9: The initial design of grating coupler with an incident angle of 10°.

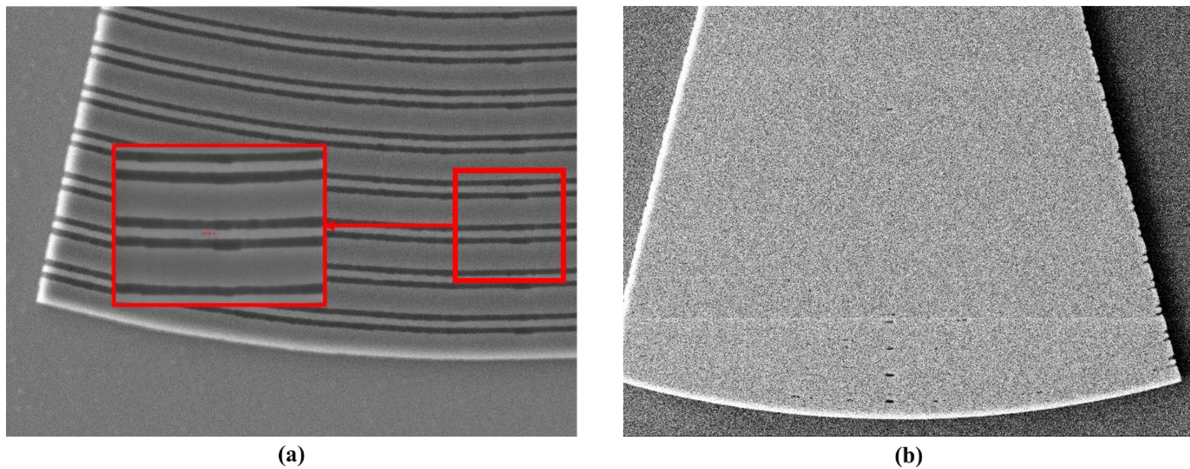


Figure 5.10: SEM image of the initial design of grating coupler (a) after exposure to E-beam, and (b) after etching process and removal after photoresist.

Most importantly, the etch depth of the grating structure was not what we desired. Because of over-exposure and over-etching after exposure, the etch depth varied from 90 nm to 120 nm according to the AFM measurement which is different from the designed etch depth of 70 nm. Figure 5.11 shows the AFM image of the grating structure. From this measurement, simulation of the grating coupler is done again, with a variation of etch depth from 70 nm to 120 nm. The transmittance of the grating coupler decreases from 48% to 10% as etch depth increases (Figure 5.12). Based on the simulation results, the insertion loss of the system due to four grating couplers increases from 12 dB to 21 dB. In addition, due to the low quality of the surface, extra insertion loss and propagation loss by the SiPh devices must be considered.

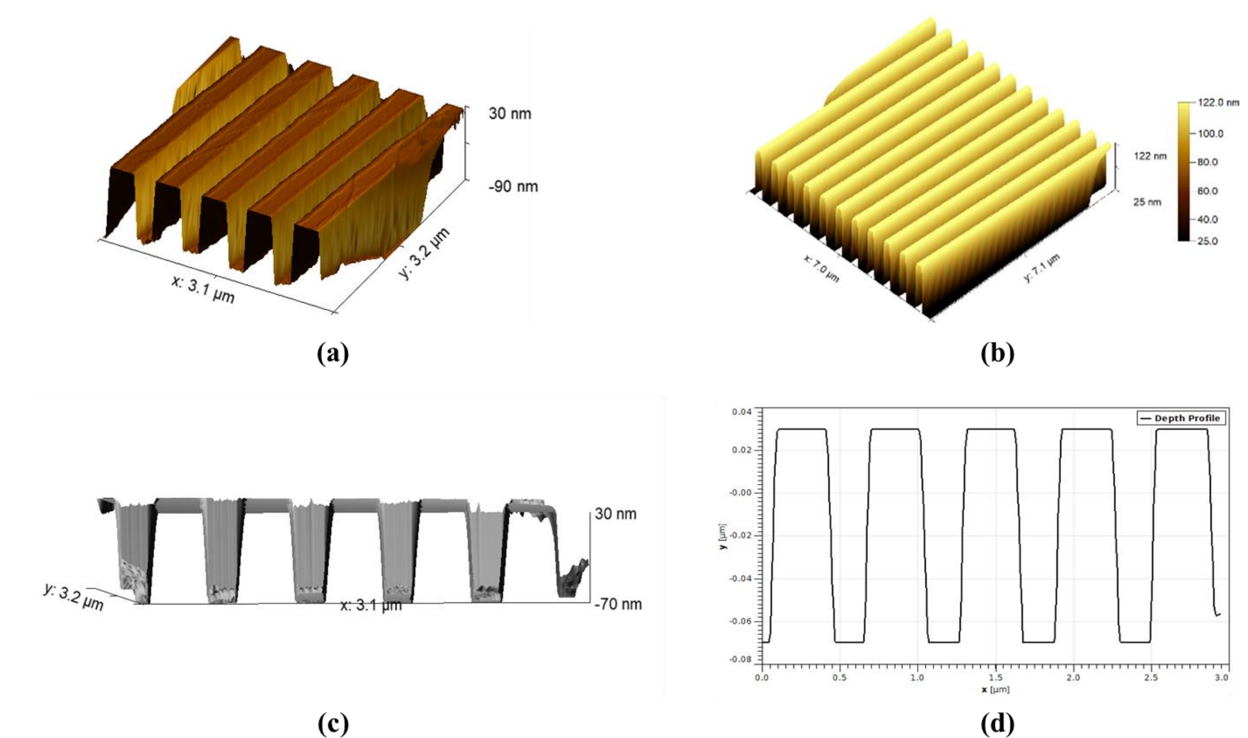


Figure 5.11: AFM image of the grating coupler with etch depth of (a) 120 nm and (b) 100 nm. (c) Side view of the grating coupler, and (d) depth profile of gratings in (b) and (c).

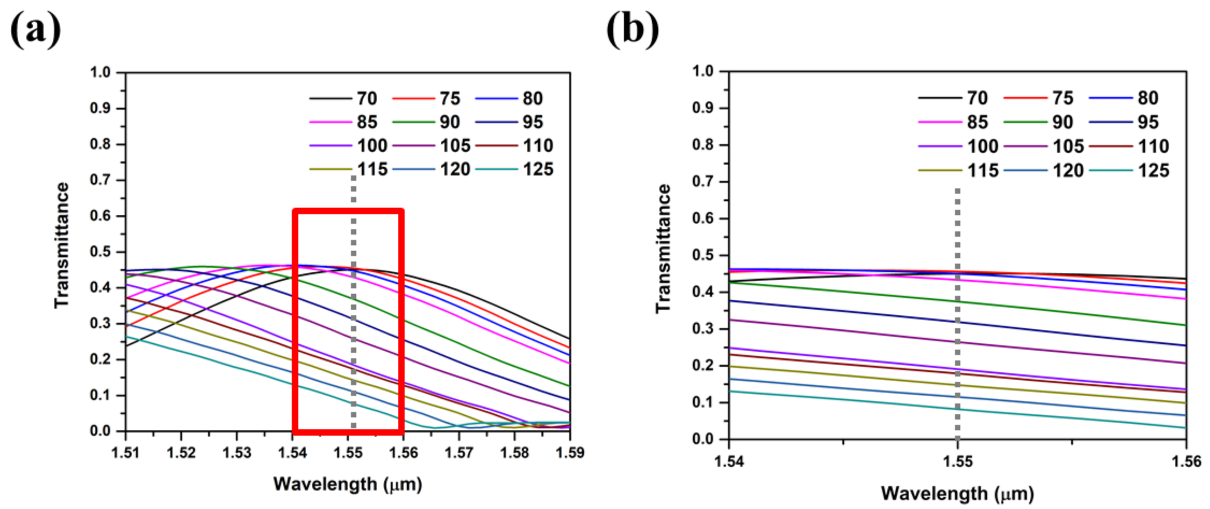


Figure 5.12: Simulation result of transmittance of the grating coupler as a function of the wavelength for different grating etch-depth.

6. CONCLUSIONS

6.1 Summary of Hybrid Optical Integrator

A hybrid optical integrator based on a silicon waveguide loop with fiber-optic components is proposed, simulated, fabricated and experimentally demonstrated. Beginning with the system architecture and the theoretical principle of the optical leaky integrator, the mathematical model of this proposed device is verified to be functional as an optical leaky integrator. Using the Lumerical software, silicon photonics components such as a grating coupler, directional coupler, Y–branches and waveguide were designed, and expected insertion loss were simulated. Based on the design, a MATLAB simulation was performed to verify the system functionality.

The proposed system was designed and constructed for two different systems: a fiber-optic integrator to demonstrate and verify the theoretical model of the optical integrator, and the other, a hybrid optical integrator with that the SiPh device to a replace the fiber components. From the experimental result of the fiber-optic integrator, the proposed system exhibits the behavior of an optical leaky integrator with a sampling period of 50 ns and FSR of 20 MHz with the optical loop length of 10 m. As optical loop length is decreased to 7.5 m, it can be observed that the sampling period of the system also decreases to 36 ns.

By implementing the SiPh device, the optical loop length is decreased from 10 m to 5 m, and it shows the decrease of the sampling period from 50 ns to 28 ns. As a result, the maximum input signal frequency increases from 1.0 MHz to 1.8 MHz with an oversampling ratio of 20X. The experimental result shows that the SiPh device can be a replacement for the optical fiber to

decrease the optical loop length. However, the power loss at each grating coupler is relatively large compared to that of the fiber cable due to the fabrication quality of the SiPh device and the alignment procedure. The driving current of the laser source and the SOA must be set to their maximum value to obtain optimized operation conditions. It is recommended to reduce the number of grating couplers in the design. The proposed design requires four grating couplers due to external optical devices. Appropriate design of an on-chip SOA, a band-pass filter and an optical isolator can eliminate two grating couplers [35]. In Figure 4.4, the grating couplers A and C can be eliminated in the case of integrated on-chip SOA, band-pass filter and optical isolator in the SiPh device. The insertion loss then decreases to at least 21 dB, which improves device power efficiency. The implementation of the external devices on the SiPh chip also decreases the fiber length within the optical loop length, leading to higher operation frequency.

6.2 Recommendations for Future Research

First, the fabrication yield rate of SiPh devices should be improved. The yield rate can be improved by using a higher uniformity of SOI wafer. In this thesis, the thickness variation of the device layer is approximately 200 nm as mentioned in Section 3.1.2, which decreases the functional area on the SOI wafer. Only a specific area on the wafer meets the requirement of the desired uniform thickness. However, if there is a larger area where the thickness of the device layer is within 220 nm ± 30 nm, the number of functional devices will increase. From the wafer thinning process, we obtained data that reveals the oxidation and etching decrease the thickness but do not affect the thickness variation or roughness. In addition, the initial thickness of the device layer also affects

the quality of E-beam lithography. As such, it is essential to buy and use an SOI wafer with lower thickness variations, ± 30 nm.

Second, improvement of the quality of fabricated devices, such as the roughness of waveguides and nanoscale structures, etch depth, minimum resolution, and corrugation of the gratings can decrease the insertion loss significantly. Due to the absence of proper equipment for E-beam lithography, the device for this thesis was fabricated at the University of Minnesota. However, from the inspection, the device shows some defects as described in Section 5.2. From SEM and AFM images, there are several factors that could increase the insertion loss of the grating coupler and propagation loss of the waveguide. According to References [15] and [16], the improvement of roughness on the waveguide decreases the propagation loss. In addition, several studies show the importance of the fabrication process and the quality of the Si structure [36]. It is possible to fabricate SiPh devices in higher quality by other cleanroom facility with more experience in SiPh processes [36]. As the quality of the fabricated devices improve, the difference between the device performance and the simulation results becomes negligible.

Last but not least, the automated alignment system can increase the experiment efficiency by reducing the difficulty of the alignment process. According to Reference [37], the automated probe system can be constructed with PXI-express Chassis, automated motion control stage, optical power meter, and software. With this system, the alignment procedure decreases from one of two hours to a few minutes. With the help of an automatic probe station, a more significant number of devices can be experimentally investigated for the same period of time.

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APPENDICES

Appendix A – Lumerical Software Simulation Procedure

In this section, a detail procedure of the Lumerical software simulation process will be explained based on the grating coupler. First, open the Lumerical FDTD and import a model or create a model as the desired structure. The Si layer and SiO_2 layer are created in the shape of a rectangle (Figure A.1(a)), and the geometry and material of each layer can be assigned by editing each rectangle structure as shown in Figure A.2. Then the grating coupler can be inserted using object library (Figure A. 1. (b)) or import STL file that is drawn by CAD software (Figure A.1(c)). The objects tree in Figure A.1(d) will show the model that is imported or created, and structure view will display red (Si) and grey (SiO_2) blocks (Figure A.3).

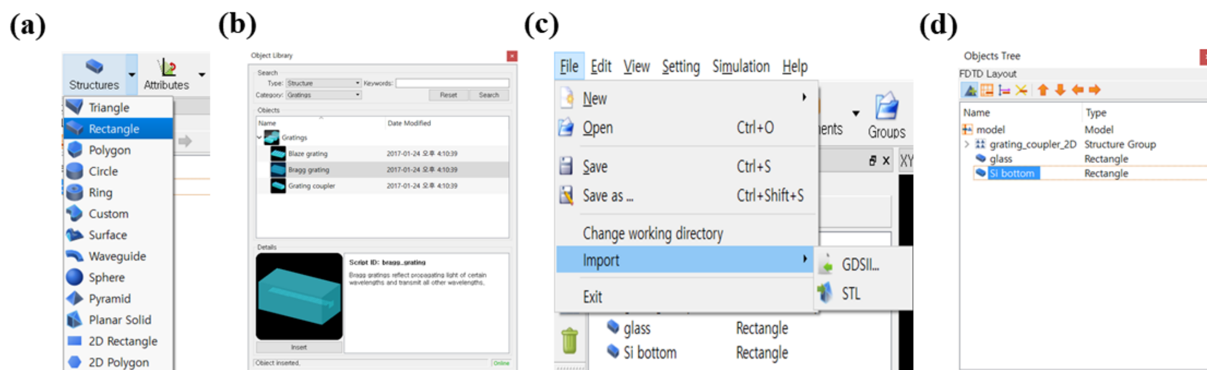


Figure A.1: Lumerical image of inserting model for the simulation setup.

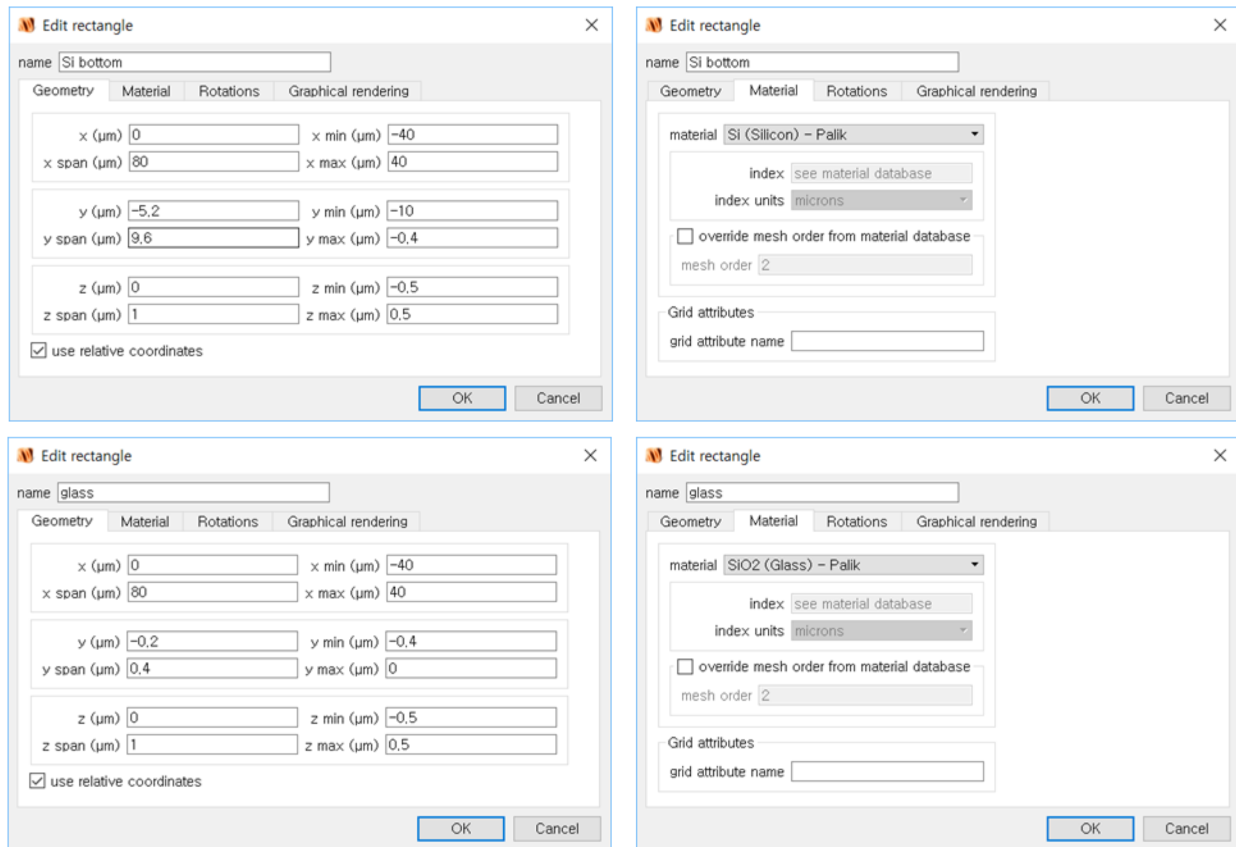


Figure A.2: Geometry and material setup for the Si and SiO_2 layers.

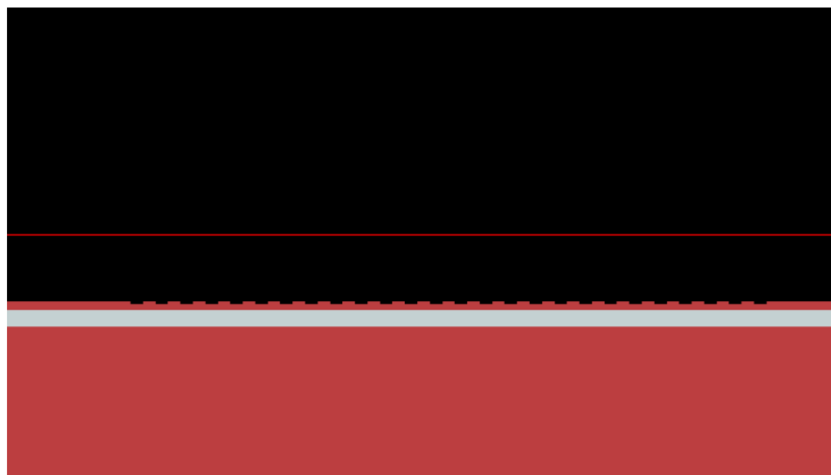


Figure A.3: Imported grating coupler into Lumerical FDTD.

After the model for the simulation is assigned, click 'Simulation → Region' and 'Port' to add FDTD simulation and I/O port for the direction of light propagation (Figure A.4 and A.7). A yellow rectangle that appeares in the XY view window as shown in Figure A.6. The simulation region, mesh setup, and wavelength can be changed depending on the interest of simulation (Figure A.5). There are two ports inserted for the simulation, port 1 for light propagation between fiber and grating coupler and port 2 for light propagation between grating coupler and waveguide. The axis and direction of two ports can be edited as shown in Figure A.7 and A.8. As the experiment is coupling light from fiber to grating coupler, or grating coupler to fiber, we introduce fiber in the simulation model. Click 'Group → Analysis' and use a script to create fiber which has a core diameter of 9 μm and a cladding diameter of 100 μm (Figure A.10). The bright blue in Figure A.11. shows the fiber is inserted to the simulation model.

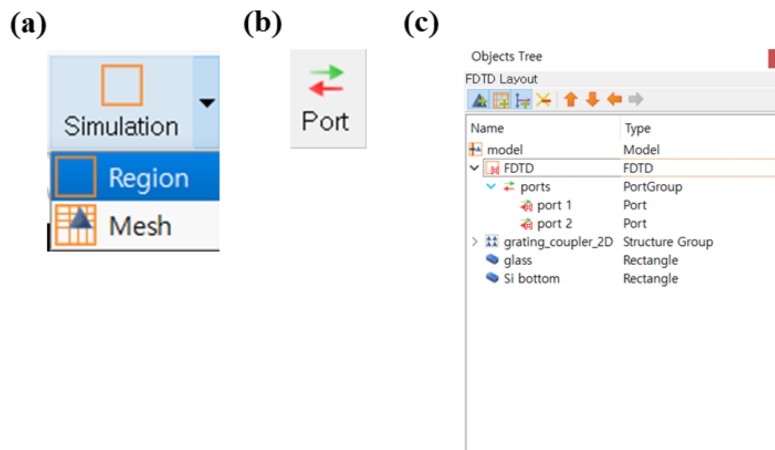
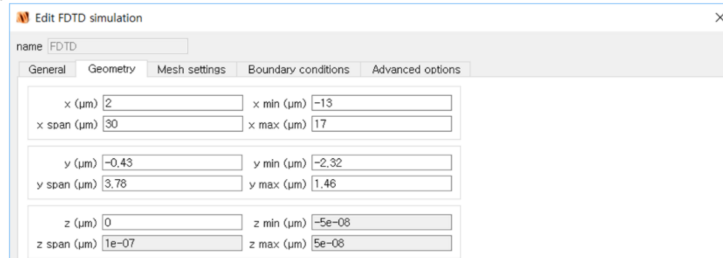
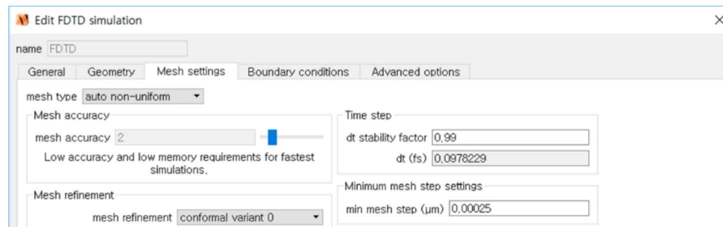


Figure A.4: Lumerical image of FDTD and port setup.

(a)



(b)



(c)

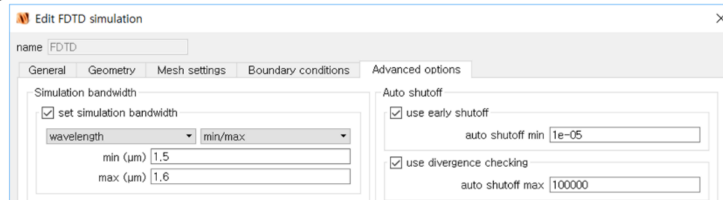


Figure A.5: FDTD simulation setup.

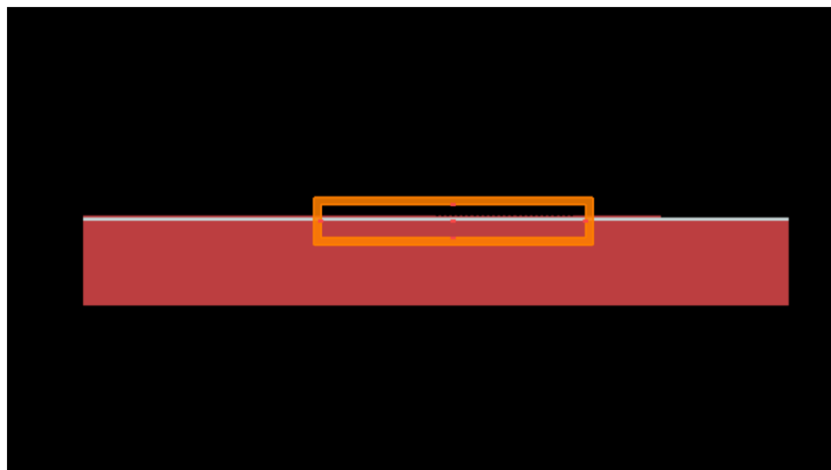


Figure A.6: Inserted FDTD simulation for the grating coupler.

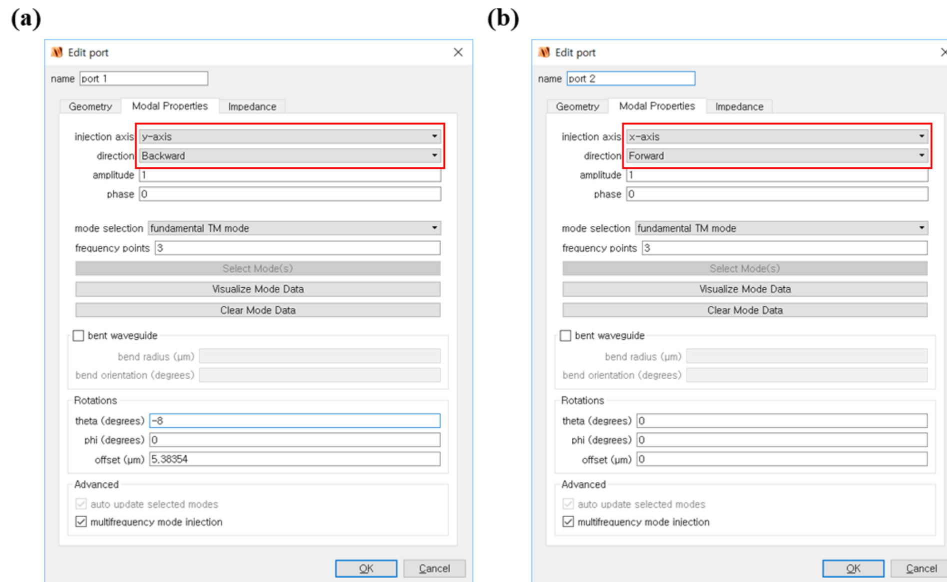


Figure A.7: Ports setup with its axis and direction.

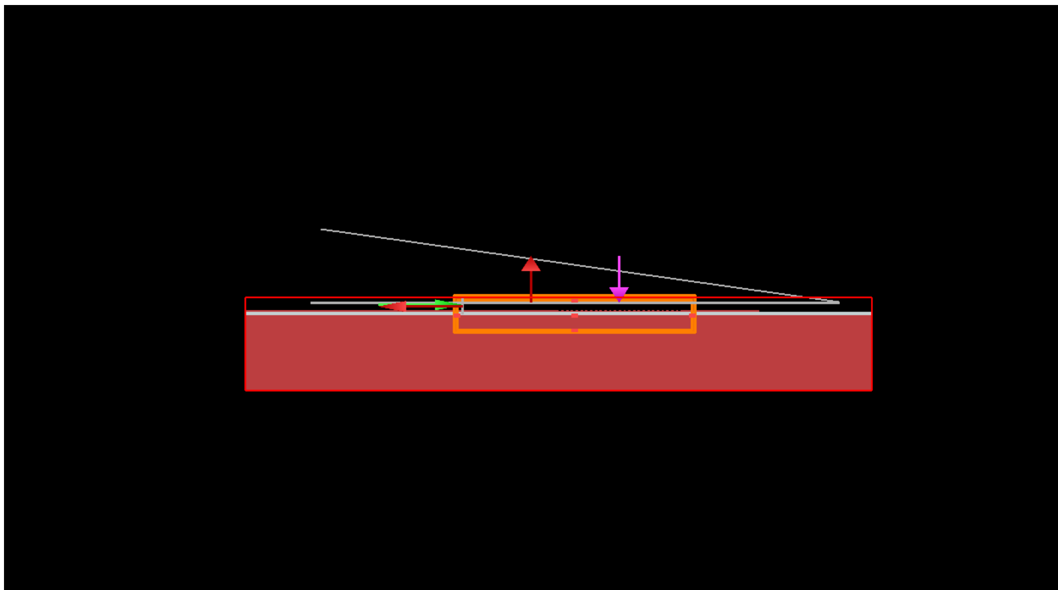


Figure A.8: Lumerical image of two ports in the simulation model (y-direction for fiber to grating coupler and x-direction for the grating coupler to waveguide).

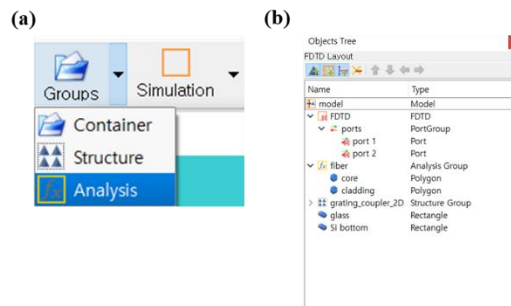


Figure A.9: Lumerical image for the insertion of fiber.

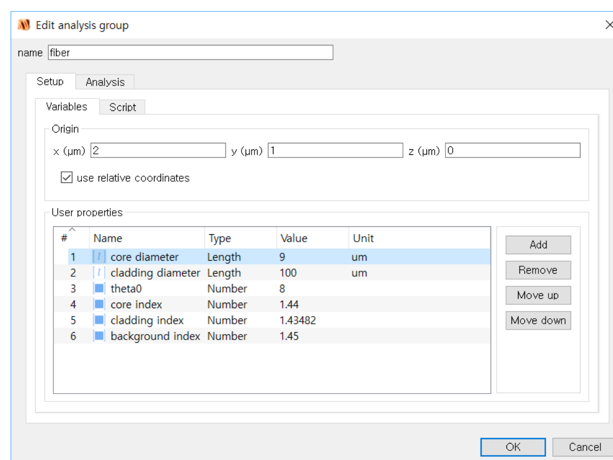


Figure A.10: Fiber geometry and properties setup.

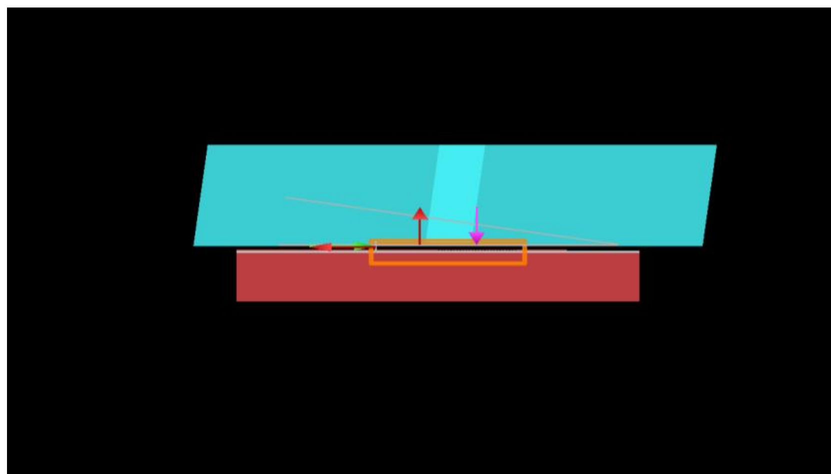


Figure A.11: Lumerical image of the inserted fiber (blue structure) for the FDTD simulation.

Two types of monitors are setup for the observation of simulation results, one for the profile monitor, and the other for the power monitor at a certain point or area. The profile monitor provides the gradient image of power distribution for a designated area, while the power monitor shows the power transmitted to a designated line-space. To verify the tranmittance of grating coupler, from the fiber to the grating coupler, or the opposite, four power monitors are inserted. The setup of the profile monitor and power monitor is shown in Figure A.13 and A.14. Figure A.15 shows the final model for the simulation of the grating coupler.

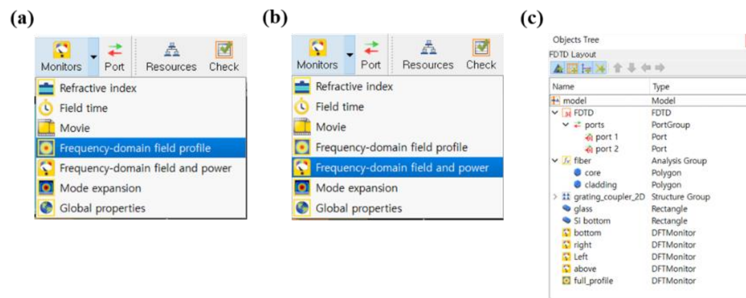


Figure A.12: Lumerical image of insertion of the monitor for simulation result.

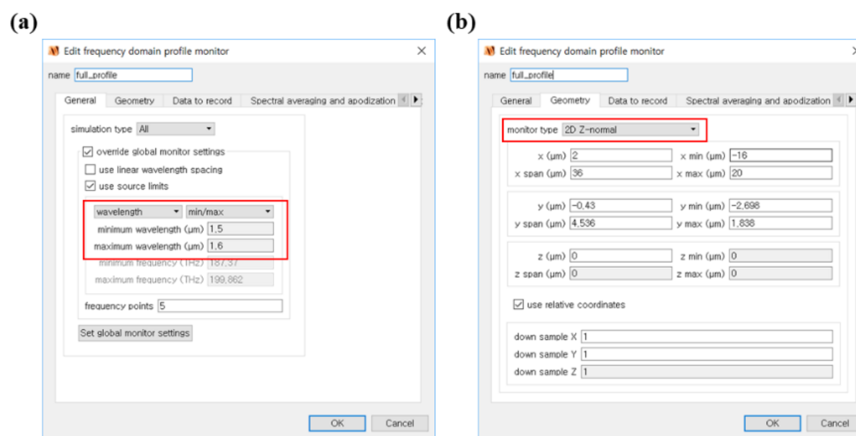


Figure A.13: Lumerical image for the frequency domain profile monitor setup.

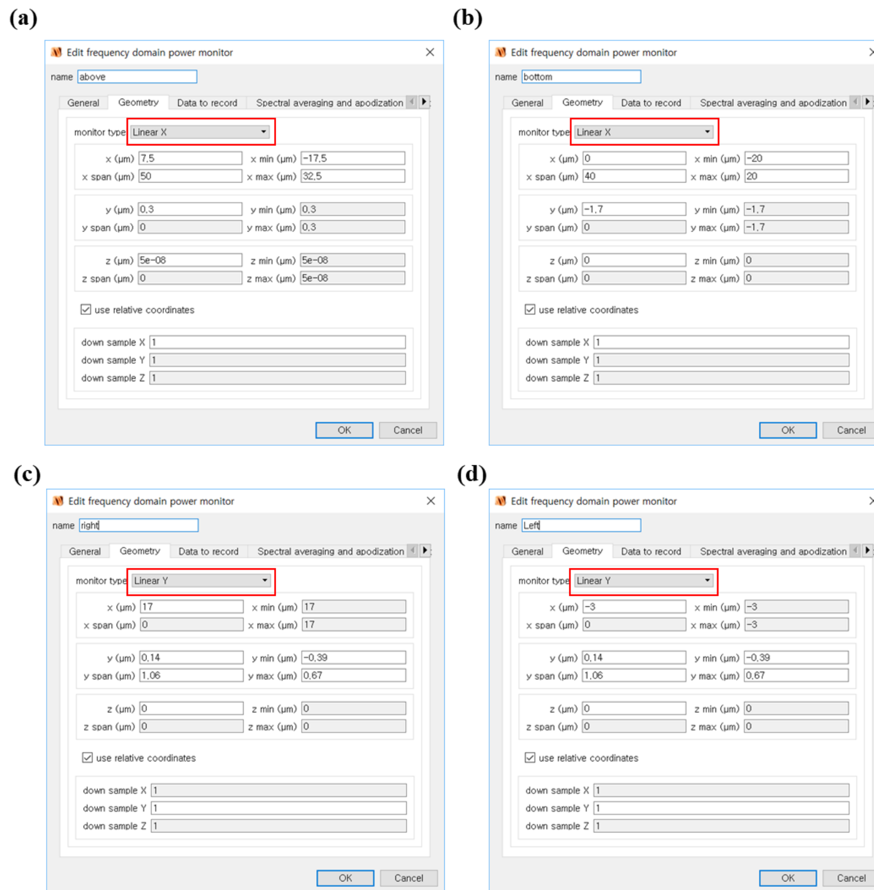


Figure A.14: Lumerical image for the frequency domain power monitor setup.

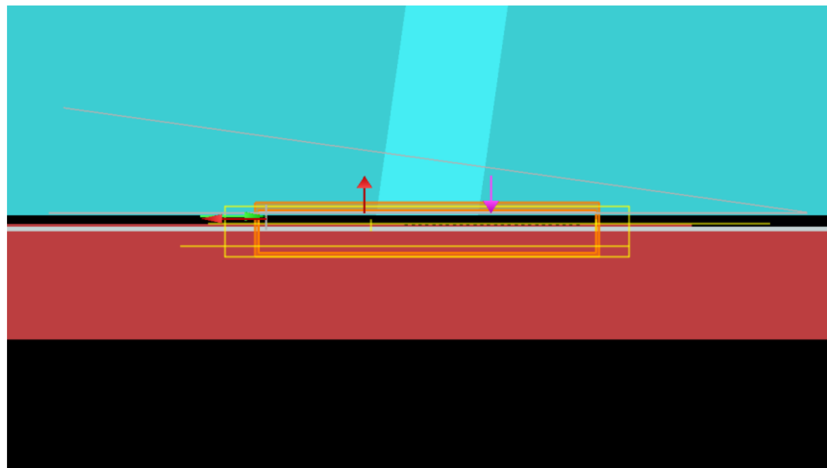


Figure A.15: The final simulation model for the grating coupler.

Appendix B – K-layout Design Procedure

The GDS file for the E-beam lithography is created by K-layout. This part includes a detail procedure of the design process including package installation and model import to the library. First, the SiEPIC package must be installed as follows:

1. Click Tool → Manage packages (Figure B.1(a))
2. Select and install the 'SiEPIC-Tools' package, 'SiEPIC-EBeam-PDK' package and 'Windows_Python_Packages_forKLayout' packages (Figure B.1(b))
3. Restart K-layout. Now the waveguide routing and design library are accessible (Figure B.2).

To utilize the functionality of the installed package for the routing waveguide, the designed component must be included in the component library of the package (SiEPIC-EBeam.gds) with pins included. It can be seen that the provided components library contains pins that enable interactive waveguide routing (Figure B.3). Components and pins in the package library are recognized, and by just clicking 'w,' the components can be connected with a designated waveguide. The below list is the procedure for how to setup a pin into a designed component and how to insert a design into the library.

1. Create a new layout, choose 'Ebeam' technology, edit 'Top cell' name (component name, for example, straight_te_gc, *etc.*) and initial window size (Figure B.4(a))
2. Select the 'Si' layer and import the designed component. If the material is not silicon, the new layer can be created depending on the design (Figure B.4(b))
3. Select 'PinRec' layer and create 'Box' with a dimension of 200 × 500 nm, or copy one of the pins from the component in package library (Figure B.5(a)).

4. Place the pin at the desired location on the design (Figure B.5(b)).
5. Open 'SiEPIC-EBeam.gds' as 'Open in the new panel' (the file is located at C:\Users\Username\KLayout\salt\siepic_ebeam_pdk\tech\EBeam\pymacros). In this case, the 'straight grating coupler' will be added to this file.
6. Create new cell and edit name (straight_te_gc).
7. Click 'Instance' (Figure B.6(a)) and select 'Local' in the library (Figure B.6(b)). The designed component can be browsed.
8. Click 'Ok' and place the component at the desired location. If the process is properly done, the component can be seen in the 'Cell' window as shown in Figure B.6(c).
9. Save the 'SiEPIC-EBeam.gds.'

After the component is added to the library, it can be added or accessible to the routing waveguide using 'Instance' → 'EBeam Library' as shown in Figure B.7. By adding custom design, the waveguide construct becomes much easier. Using the 'Path' function, set the thickness of the waveguide (Figure B.8(a)) and locate the waveguide as desired. One of the advantages of the package is that the waveguide does not need to be accurately aligned at the end of the component. As shown in Figure B.9(a), even though there is a gap between the waveguide and component, select the waveguide and click 'w' to automatically arrange the waveguide to the pin of the component. This function also provides automatic bend radius in case of a bent waveguide.

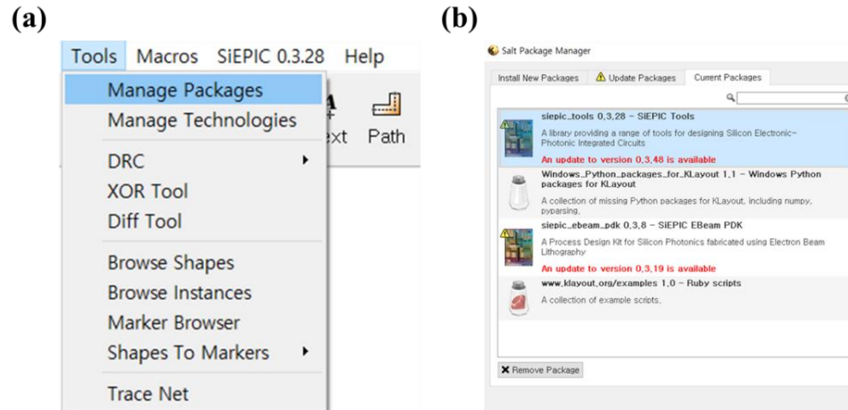


Figure B.1: Installation of SiEPIC package for K-Layout.

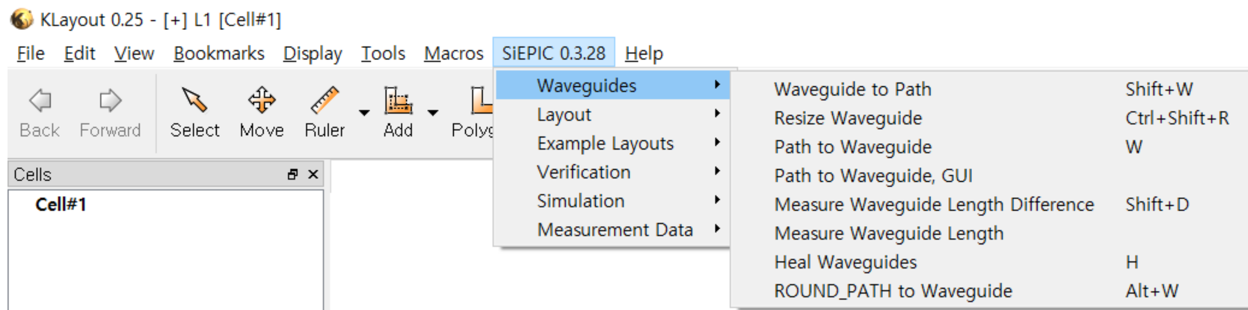


Figure B.2: Installed SiEPIC package and its routing function for the waveguide.

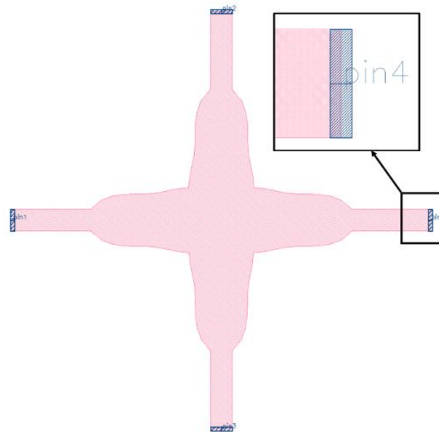


Figure B.3: Example of the component that includes pins for routing waveguide.

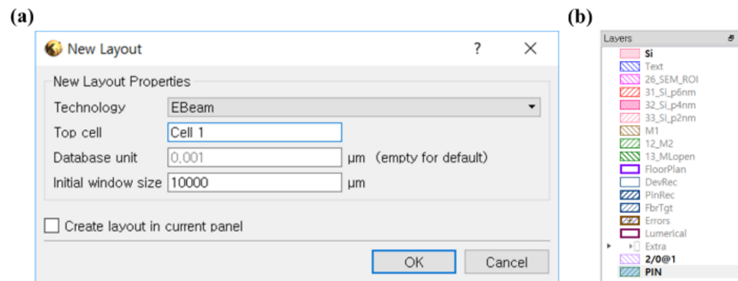


Figure B.4: (a) New layout window and (b) Layer window that shows basic layers.

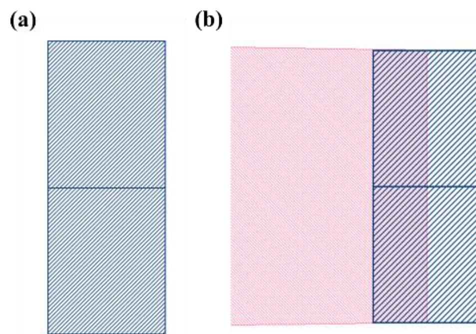


Figure B.5: (a) K-layout image of a pin and (b) placement of the pin at the desired location.

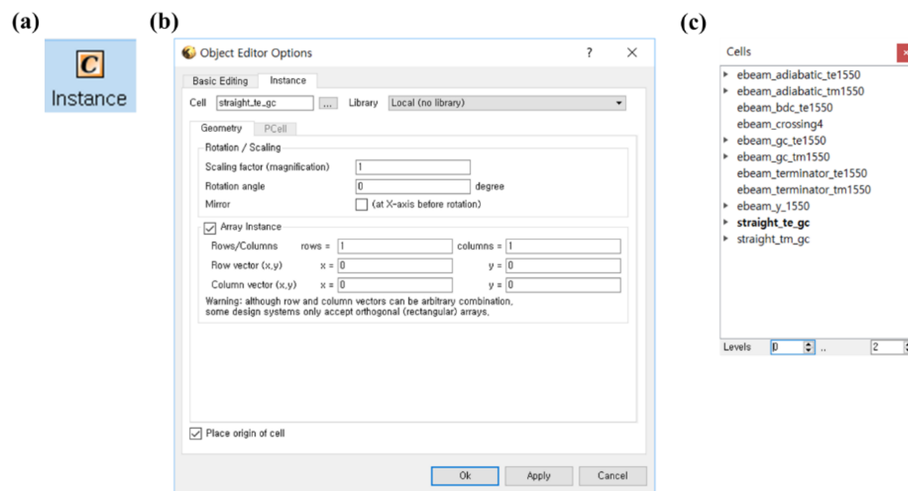


Figure B 6: (a) Instance and (b) instance window to add a design into the cell. (c) The cell window shows that 'straight_te_gc' is inserted in the package library.

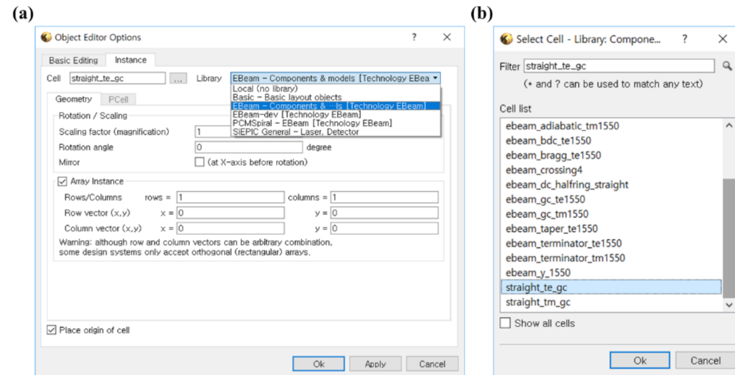


Figure B.7: (a) 'EBeam' library in the package and (b) list of components in the library with the inserted component.

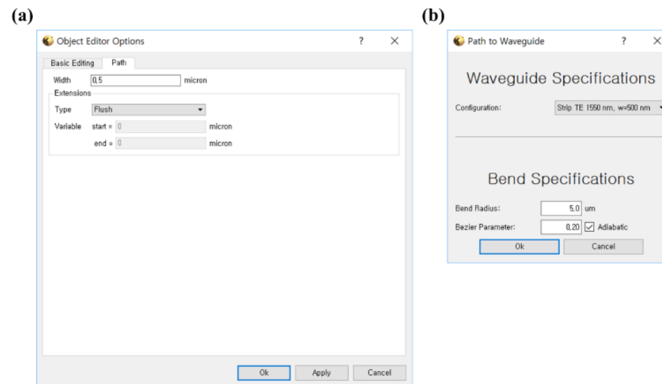


Figure B.8: (a) 'Path' function with specific waveguide width and (b) waveguide function 'w' of the package.

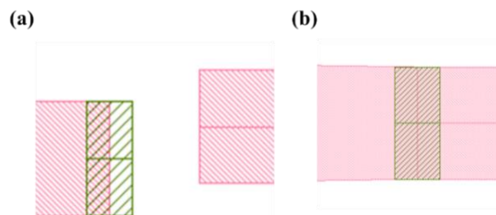


Figure B.9: (a) Misaligned waveguide and component and (b) perfectly fitted waveguide to a component by using 'w' function of the package without overlap.

Appendix C – Matlab Code for Simulation Model

C.1. Grating coupler

```
n_periods = ceil(%target length%/pitch); fill_width = pitch*%duty cycle%;
etch_width = pitch*(1-%duty cycle%); L = n_periods*pitch + etch_width;
if(%etch depth% > %h total%) { %etch depth% = %h total%;}
addrect;
set("name","input waveguide");
set("x min",-%input length%); set("x max",0); set("y min",0); set("y max",%h total%);
if(%etch depth% < %h total%) {addrect; set("name","lower layer");
set("x min",0); set("x max",L); set("y min",0); set("y max",%h total%-%etch depth%);}
addrect;
set("name","output waveguide");
set("x min",L); set("x max",L+%output length%); set("y min",0); set("y max",%h total%);
#add grating
for(i=1:n_periods){ addrect; set("name","post");
set("x min",pitch*(i-1)+etch_width); set("x max",pitch*i);
set("y min",%h total%-%etch depth%); set("y max",%h total%);}
selectall; set("material",material);
if(get("material")=="<Object defined dielectric>")
{ set("index",index); }
set("z",0); set("z span",1e-6);
```

C.2. Fiber

```
?theta = asin( %background index%*sin(theta0*pi/180)/%core index% )*180/pi;
r1 = %core diameter%/2; r2 = %cladding diameter%/2;
if(theta >    89) { theta = 89; } if(theta < -89) { theta = -89; }
thetarad = theta*pi/180; L = 20e-6/cos(thetarad);
V1 = [ -r1/cos(thetarad), 0; r1/cos(thetarad), 0; r1/cos(thetarad)+L*sin(thetarad), L*cos(thetarad);
-r1/cos(thetarad)+L*sin(thetarad), L*cos(thetarad)];
V2 = [ -r2/cos(thetarad), 0; r2/cos(thetarad), 0; r2/cos(thetarad)+L*sin(thetarad), L*cos(thetarad);
-r2/cos(thetarad)+L*sin(thetarad), L*cos(thetarad)];
select("core"); set("vertices",V1); set("index",%core index%); select("cladding");
set("vertices",V2); set("index",%cladding index%);
span = 15*r1;
```

Appendix D – Matlab Code for Waveguide

D. Mode parameters and effective index calculation of 1D slab waveguide

```
function [nTE,nTM,TEparam,TMparam] = wg_1D_analytic (lambda, t, n1, n2, n3)

k0 = 2*pi/lambda; b0 = linspace( max([n1 n3])*k0, n2*k0, 1000);

b0 = b0(1:end-1);

te0=TE_eq(b0,k0,n1,n2,n3,t);

intervals=(te0>=0)-(te0<0); izeros=find(diff(intervals)<0); X0=[b0(izeros); b0(izeros+1)]';

[nzeros,scrap]=size(X0);

for i=1:nzeros

nTE(i)=fzero(@(x) TE_eq(x,k0,n1,n2,n3,t),X0(i,:))/k0;

[TEparam(i,1),TEparam(i,2),TEparam(i,3),TEparam(i,4)]= TE_eq(nTE(i)*k0,k0,n1,n2,n3,t);

end

nTE=nTE(end:-1:1); TEparam=TEparam(end:-1:1,:);

function [te0,h0,q0,p0]=TE_eq(b0,k0,n1,n2,n3,t)

h0 = sqrt( (n2*k0)^2 - b0.^2 ); q0 = sqrt( b0.^2 - (n1*k0)^2 ); p0 = sqrt( b0.^2 - (n3*k0)^2 );

te0 = tan( h0*t ) - (p0+q0)./h0./(1-p0.*q0./h0.^2);
```