Development and Verification of Multi-Level Sub-Meshing Techniques of PEEC to Model High-Speed Power and Ground Plane-Pairs of PCBs

Master Thesis Defense

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PDN, why do we care?

Figure 1: A full PDN [1]
Figure 2: Extract a plane pair, once we do the plane-pair problem for each layer, we can cascade layers as part of the overall PCB simulation.
Goal

- Develop a new efficient approach to model complex multilayer PCB with many vias
- Develop time and frequency-domain solvers
- Design guidelines
- Placement and number of decoupling capacitors
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- Develop a new efficient approach to model complex multilayer PCB with many vias
- Develop time and frequency-domain solvers
- Design guidelines
- Placement and number of decoupling capacitors
- Decoupling capacitors leave a footprint (Poles and Zeros) in the impedance profile
Motivation, why PPP (Plane-Pair PEEC)?

- Existing methods for PDN problems:
  EM solutions: FDTD, FEM, Integral Equation models
  conventional full-wave solution, too slow

- Analytical solution: Cavity model
  depends on the propagating modes, number of cavities

- Complexity increases with the number of vias

- PPP has nature advantages over other methods
  - Fast and accurate
  - PEEC models electric-field interactions as capacitances and magnetic-field interactions as inductances
  Conventional SPICE- like circuit solvers
  Integral eq. → KCLs and KVLs
PEEC equivalent circuit of a plane-pair
Advantages

- Speed-up due to matrix sparsification
  - Orthogonal cells guarantee no X-Y coupling
  - Take advantages of the opposing currents $\rightarrow$ Difference inductance model [2]
  - Mutual terms fall off quickly

Conclusion: Matrix can be sparsified which will speed up simulations
Advantages

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  - Orthogonal cells guarantee no X-Y coupling
  - Take advantages of the opposing currents $\rightarrow$ Difference inductance model [2]
  - Mutual terms fall off quickly

Conclusion: Matrix can be sparsified which will speed up simulations

- Speed-up due to multi-level meshing, fewer unknowns
Advantages

- PEEC model is based on finite sections partial inductances applicable to any line length
- Better than TL’s, per-unit-length values, which assumes an infinitely long line
- → more accurate at discontinuities
  e.g., hole or edges of the board
Advantages

- PEEC model is based on finite sections partial inductances applicable to any line length
  Better than TL’s, per-unit-length values, which assumes an infinitely long line
  → more accurate at discontinuities
  e.g., hole or edges of the board
- Integral eq. model for partial inductances
  Differential eq. model for partial capacitances
Decoupling capacitor models used for different solutions

- Inductance solution only: Insert short or ESL
- Time domain solution: Insert ESR, ESL and C
- Frequency domain solution: ESR, ESL
Partial inductance

\[ \vec{B} = \nabla \times \vec{A} \]

\[ L_{\text{loop}} = \frac{\Psi}{I} = \frac{\int \int_{s} \vec{B} \cdot d\vec{s}}{I} = \oint_{C} \vec{A} \cdot d\vec{l} \]
Partial inductance

\[ L_{\text{loop}} = \oint _{C} \vec{A} \cdot d\vec{l} \]

\[ = \int_{C_1} \vec{A} \cdot d\vec{l} + \int_{C_2} \vec{A} \cdot d\vec{l} + \int_{C_3} \vec{A} \cdot d\vec{l} + \int_{C_4} \vec{A} \cdot d\vec{l} \]

Partial self inductance of a segment of a conductor is defined as

\[ L_{pi} = \frac{\int_{C_i} \vec{A} \cdot d\vec{l}}{I_i} \]
Simplest model for inductive behavior [2, 3]

- Each of the connections includes a partial inductance
- N1 is shorted due the decoupling capacitor
- Inject a current into N4 due to IC, switching or AC source at IC
- Input Inductance $= \frac{V_{N4}}{sI_s}$

Let’s write a KCL,

$$I_{x1} + I_{y1} + I_{sh} = 0$$

and a KVL as well

$$V_{N1} - V_{N2} = sL_{p11}I_{x1} + sL_{p12}I_{x2}$$
Simplest model for inductive behavior \[2, 3\]

- Each of the connections includes a partial inductance
- N1 is shorted due the decoupling capacitor
- Inject a current into N4 due to IC, switching or AC source at IC
- Input Inductance \( \frac{V_{N4}}{sI_s} \)

\[
\begin{bmatrix}
0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 \\
0 & 0 & 0 & 0 & -1 & 0 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & -1 & 0 & -1 & 0 \\
1 & -1 & 0 & 0 & -sL_{px11} & -sL_{px12} & 0 & 0 & 0 \\
0 & 0 & 1 & -1 & -sL_{px21} & -sL_{px22} & 0 & 0 & 0 \\
1 & 0 & -1 & 0 & 0 & 0 & -sL_{py11} & -sL_{py12} & 0 \\
0 & 1 & 0 & -1 & 0 & 0 & -sL_{py21} & -sL_{py22} & 0 \\
1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
V_{N1} \\
V_{N2} \\
V_{N3} \\
V_{N4} \\
I_{x1} \\
I_{x2} \\
I_{y1} \\
I_{y2} \\
I_{sh}
\end{bmatrix}
= \begin{bmatrix}
0 \\
0 \\
0 \\
0 \\
0 \\
0 \\
0 \\
0 \\
0
\end{bmatrix}
Simplest model for inductive behavior [2, 3]

- Each of the connections includes a partial inductance
- N1 is shorted due to the decoupling capacitor
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\[
\begin{bmatrix}
0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 \\
0 & 0 & 0 & 0 & -1 & 0 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & -1 & 0 & -1 & 0 \\
1 & -1 & 0 & 0 & -sL_{px11} & -sL_{px12} & 0 & 0 & 0 \\
0 & 0 & 1 & -1 & -sL_{px21} & -sL_{px22} & 0 & 0 & 0 \\
1 & 0 & -1 & 0 & 0 & 0 & -sL_{py11} & -sL_{py12} & 0 \\
0 & 1 & 0 & -1 & 0 & 0 & -sL_{py21} & -sL_{py22} & 0 \\
1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & Zc
\end{bmatrix}
\begin{bmatrix}
V_{N1} \\
V_{N2} \\
V_{N3} \\
V_{N4} \\
I_{x1} \\
I_{x2} \\
I_{y1} \\
I_{y2} \\
I_{sh}
\end{bmatrix} = \begin{bmatrix}
0 \\
0 \\
0 \\
I_s \\
0 \\
0 \\
0 \\
0 \\
0
\end{bmatrix}
\]
With capacitance and conduction loss added

\[
sC = \begin{bmatrix}
  sC_{11} & 0 & 0 & 0 \\
  0 & sC_{22} & 0 & 0 \\
  0 & 0 & sC_{33} & 0 \\
  0 & 0 & 0 & sC_{44}
\end{bmatrix}
\]

\[
A = \begin{bmatrix}
  1 & 0 & 1 & 0 \\
 -1 & 0 & 0 & 1 \\
 0 & 1 & -1 & 0 \\
 0 & -1 & 0 & -1
\end{bmatrix}
\]

\[
-sL - R = \begin{bmatrix}
  -sL_{px11} - Rx_{11} & -sL_{px12} & 0 & 0 \\
  -sL_{px21} & -sL_{px22} - Rx_{22} & 0 & 0 \\
  0 & 0 & -sL_{py11} - Ry_{11} & -sL_{py12} \\
  0 & 0 & -sL_{py21} & -sL_{py22} - Ry_{22}
\end{bmatrix}
\]

Generalized MNA matrix representation:

\[
\begin{bmatrix}
  sC & A^T \\
  A & -sL - R
\end{bmatrix}
\begin{bmatrix}
  V_n \\
  I_b
\end{bmatrix}
= \begin{bmatrix}
  I_s \\
  0
\end{bmatrix}
\]
Difference Inductance Model

Define the difference inductance as the coupling of any two sections k and m, $L_{skm}$

- Currents in opposite directions
- Inductive coupling between sections decays fast

$$V_{sk} = V_a - V_b = sI_m(L_{pkm} - L_{pk'm'} + L_{p'km'} - L_{p'k'm})$$

$$L_{skm} = \frac{V_{sk}}{sI_m} = 2(L_{pkm} - L_{pk'm'})$$
Using Taylor series expansion under the condition that $h \ll r_{km}$, keeping terms to first-order, we have

$$L_{skm'} \approx \frac{\mu_0}{4\pi} \frac{\Delta x_k \Delta x_m (1 - \frac{h^2}{2r_{km}^2})}{r_{km}}$$

and,

$$L_{skm} = 2(L_{pkm} - L_{pkm'}) = \frac{\mu_0}{4\pi} \frac{\Delta x_k \Delta x_m h^2}{r_{km}^3}$$
Difference Inductance Model

\[ L_{pkm} = \frac{\mu_0}{4\pi} \frac{\Delta x_k \Delta x_m}{r_{km}} \quad \quad L_{pkm'} = \frac{\mu_0}{4\pi} \frac{\Delta x_k \Delta x_m}{r_{km'}} = \frac{\mu_0}{4\pi} \frac{\Delta x_k \Delta x_m}{r_{km} \sqrt{1 + \frac{h^2}{r_{km}^2}}} \]

Using Taylor series expansion under the condition that \( h \ll r_{km} \),
keeping terms to first-order, we have

\[ L_{skm'} \approx \frac{\mu_0}{4\pi} \frac{\Delta x_k \Delta x_m(1 - \frac{h^2}{2r_{km}^2})}{r_{km}} \]

and,

\[ L_{skm} = 2(L_{pkm} - L_{pkm'}) = \frac{\mu_0}{4\pi} \frac{\Delta x_k \Delta x_m h^2}{r_{km}^3} \]

\( L_{skm} \) decays fast, on the order of \( 1/r^3 \)
Simplify diff. inductances \( \rightarrow \) Faster evaluating mutual couplings
Fast decay of mutual coupling

\[ L_{n_k} = \frac{L_{s_{km}}}{L_{s_{kk}}} = \frac{\mu_0}{4\pi} \frac{\Delta x_k \Delta x_m h^2}{r_{km}^3 L_{s_{kk}}} \]

\[ 10^{-3} \text{ per decade implies } 1/r^3 \]
3D plots of current density at vias

Figure 3: Close via spacing

Figure 4: Far via spacing

Currents crowd near vias with a high spatial rate of change.
Multi-level sub-meshing

Use orthogonal cells. Sub-meshing around the via.
KCL weighting for sub-meshing

We subdivide the current so that no non-orthogonal cells are used.

**Type I Node**
\[
V_{G6} s C_{G6} + 0.75 I_{G6,G2} + I_{G6,S6} + I_{G6,S3} + 0.75 I_{G6,G5} = 0
\]

**Type II Node**
\[
V_{S3} s C_{S3} + 0.25 I_{G6,G2} + 0.25 I_{G7,G3} + I_{S3,S7} + I_{S3,G7} + I_{S3,G6} = 0
\]

**Type III Node**
\[
V_{G7} s C_{G7} + 0.5 I_{G7,G3} + I_{G7,S8} + I_{G7,S4} + I_{G7,S3} = 0
\]

**Type IV: G8**
\[
V_{G8} s C_{G8} + \frac{2}{3} I_{G8,S1} + I_{G8,S10} + I_{G8,S5} + \frac{2}{3} I_{G8,S4} = 0
\]

**Type V: S1**
\[
V_{S1} s C_{S1} + I_{S1,G4} + I_{S1,G8} + I_{S1,S2} + 0.25 I_{G4,G3} + \frac{1}{3} I_{G8,S4} = 0
\]
I. Introduction

II. Problem Statement

III. Methodology

IV. Results

V. Conclusion

References
Speed-up up to three-level sub-mesh

Table 1: Comparison between sub- and uniform mesh methods with an 80mmx80mm board

<table>
<thead>
<tr>
<th></th>
<th>Unknowns</th>
<th>L(pH)</th>
<th>Time(sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CST</td>
<td>N\A</td>
<td>345.7</td>
<td>N\A</td>
</tr>
<tr>
<td>Uni-mesh</td>
<td>77404</td>
<td>349.3</td>
<td>172.0</td>
</tr>
<tr>
<td>1 Sub-mesh</td>
<td>20108</td>
<td>355.7</td>
<td>13.6</td>
</tr>
<tr>
<td>2 Sub-mesh</td>
<td>6836</td>
<td>357.5</td>
<td>2.5</td>
</tr>
<tr>
<td>3 Sub-mesh</td>
<td>3852</td>
<td>358.5</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Figure 5: Uniform mesh

Figure 6: three-level sub-mesh
Figure 7: Run time comparison based on uniform and sub-mesh configurations.

Now, we can solve problem involving boards as large as 20cm x 20cm.
\[ i_C = C \frac{d(V_k - V_l)}{dt} \]
\[ v_L = L \frac{di_L}{dt} + Ri_L \]
\[ \alpha \frac{dx_p}{dt} = k_p x_p + k_{p-1} x_{p-1} + k_{p-2} x_{p-2} - \beta \frac{dx_{p-1}}{dt} \]

**Table 2: Numerical integration methods**

<table>
<thead>
<tr>
<th>Integration Method</th>
<th>( k_p )</th>
<th>( k_{p-1} )</th>
<th>( k_{p-2} )</th>
<th>( \alpha )</th>
<th>( \beta )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Forward Euler</td>
<td>1/( h_p )</td>
<td>-1/( h_p )</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Backward Euler 1st order</td>
<td>1/( h_p )</td>
<td>-1/( h_p )</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Backward Euler 2nd order</td>
<td>1.5/( h_p )</td>
<td>-2/( h_p )</td>
<td>1/2( h_p )</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
Time domain MNA formulation

Time domain KVL: at time $p$, node $n$

$$C_n \frac{dV_n}{dt} + \sum_{i \text{ from node } n} i_b = Is$$

$$C_n k_p V_n^{(p)} + \sum_{i \text{ from node } n} i_b^{(p)} = C_n k_{p-1} V_n^{(p-1)} + C_n k_{p-2} V_n^{(p-2)} + Is^{(p)}$$

Time domain KCL: at time $p$, branch $m$, node $l$ to $k$

$$V_l - V_k = \sum_{\text{all } k \text{ mutual to } m} L_p m \frac{d i_m}{dt} + R_m i_m + \sum_{\text{all } k \text{ mutual to } m} L_p km \frac{d i_k}{dt}$$

$$V_l^{(p)} - V_k^{(p)} = k_p L_p m i_m^{(p)} - R_m i_m^{(p)} - k_p \sum_{\text{all } k \text{ mutual to } m} L_p km i_k^{(p)}$$

$$= - L_p m k_{p-1} i_m^{(p-1)} - k_{p-2} \sum_{\text{all } k \text{ mutual to } m} L_p km i_k^{(p-2)}$$
Time domain MNA formulation

MNA matrix in the frequency domain,

\[
\begin{bmatrix}
  sC & A^T \\
  A & -sL - R
\end{bmatrix}
\begin{bmatrix}
  V_n \\
  I_b
\end{bmatrix} =
\begin{bmatrix}
  I_s \\
  0
\end{bmatrix}
\]

MNA matrix in the time domain,

\[
\begin{bmatrix}
  k_pC & A^T \\
  A & -k_pL - R
\end{bmatrix}
\begin{bmatrix}
  V^{(p)} \\
  I^{(p)}
\end{bmatrix} =
\begin{bmatrix}
  Ck_{p-1}V^{(p-1)} + Ck_{p-2}V^{(p-2)} \\
  -Lk_{p-1}I^{(p-1)} - Lk_{p-2}I^{(p-2)}
\end{bmatrix}
+ \begin{bmatrix}
  I_s^{(p)} \\
  0
\end{bmatrix}
\]
Instantaneous time impedance validation [4]

- Board size: 50x50mm
- Plane separation: h=0.6mm
- Capacitor: 1uF, ESR=0.1Ω and ESL=0.5nH
- Unit step with 20ps rise time, the worst case
A typical IC waveform

- A triangle current pulse
- Rise time: 1ns
- Fall time: 1ns
- Amplitude: 1A
Time domain animation

- A triangle current pulse
- Rise time: 1ns
- Fall time: 1ns
- Amplitude: 1A
Impedance sweep validation

1. Board size 50mm × 50mm
2. Plane separation h = 0.254mm (10mil)
3. Via diameter = 0.25mm
4. Short is at (25, 12.5); source is at (25, 37.5)
5. $\varepsilon_r = 4.3; \tan \delta = 0.025; \sigma = 5.96 \times 10^7 S/m$

Figure 8: Impedance frequency spectrum
Inductance example – Ring pattern

Figure 9: Ring pattern

<table>
<thead>
<tr>
<th>Case</th>
<th>Decap number</th>
<th>Decap distance (radius r)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case1</td>
<td>1, 2, 4, 8, 16, 32</td>
<td>12.7mm / 0.5”</td>
</tr>
<tr>
<td>Case2</td>
<td>1, 2, 4, 8, 16, 32</td>
<td>25.4mm / 1”</td>
</tr>
<tr>
<td>Case3</td>
<td>1, 2, 4, 8, 16, 32</td>
<td>50.8mm / 2”</td>
</tr>
<tr>
<td>Case4</td>
<td>1, 2, 4, 8, 16, 32</td>
<td>76.2mm / 3”</td>
</tr>
</tbody>
</table>
Inductance example – Ring pattern results

**Figure 10:** Ring pattern

**Figure 11:** Inductance plot
Summary

PPP

- PPP is very flexible, can be use to build block solution
- Matrix stamping is very flexible and efficient, time domain is faster than frequency domain
- Plane-pair, stack layers to form a complex PDN

Applications

- SI/PI
  - PDN design guideline, helps designer makes informed decisions, expecting the performance of the design

Future work

Create a simulation tool for designers which includes frequency-domain and time-domain solvers together with optimization for component placement
References


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The End

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